



MIPI Alliance Standard for Display Bus Interface v2.0

MIPI Board approved 16 November 2005

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MIPI Alliance Standard for Display Bus Interface

Version 2.00 – 29 November 2005

MIPI Board Approved 16-Nov-2005

Further technical changes to DBI are expected as work continues in the Display Working Group

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71 MIPI Alliance Standard for Display Bus Interface

72 1 Overview

73 This document describes Display Bus Interface (DBI), which is used for display modules. DBI can be
74 configured for 1, 2, 8, 9 or 16 data signals.

75 This document defines the interface parameters outlined below for both the host processor and display
76 module.

- 77 • Electrical
- 78 • Timings
- 79 • Protocol examples
- 80 • Measurement methods
- 81 • Color coding
- 82 • Command set to control display behaviors

83 1.1 Scope

84 The Display Bus Interface specification defines the electrical and logical interfaces for mobile device host
85 processors and display modules. Logical control of the display module functional blocks such as power
86 supply, timing generator and display drivers is also within the scope of this document. The design of the
87 functional blocks is not within the scope of this specification.

88 1.2 Purpose

89 The Display Bus Interface specification is used by manufacturers to design products that adhere to MIPI
90 specifications for mobile device processor and display interfaces.

91 Implementing the DBI standard reduces the time-to-market and design cost of mobile devices by
92 simplifying the interconnection of products from different manufacturers. In addition, adding new features
93 such as larger or additional displays to mobile devices is simplified due to the extensible nature of the MIPI
94 specifications.

95 2 Terminology

96 2.1 Definitions

97 **Command:** Digital information used to control display behavior and to identify the connected display
98 module

99 **Data:** Digital image data stored in the frame memory or numerical information to define the display
100 module behavior accompanied with a command

101 **Display Controller:** Isolated IC silicon chip or integrated functional block in the host processor to control
102 a display module; may or may not include frame memory

103 **Display Device:** Functional device which can show image, such as Liquid Crystal Displays

104 **Display Driver IC:** IC silicon chip in a display module used to control the display device; may or may not
105 include frame memory

106 **Display Glass:** Same as display device, coming from material name

107 **Display Module:** Functional module to show image on it, can consists of display device, display driver IC,
108 other peripheral components and circuits and display interface

109 **Display Panel:** Same as Display Device, coming from the physical outward appearance of the display
110 device

111 **Frame Memory:** Memory device integrated in a display driver IC or display controller in order to provide
112 image data for refreshing the display device. Full-frame memory provides a full screen area of image data
113 while partial-frame memory only provides memory for a portion of the screen area.

114 **Type 1 Display Architecture:** One of the defined display module architectures. In DSI, DBI, DPI, and
115 DCS, a display module architecture in which a display module includes a display device, display driver IC,
116 full-frame memory, registers, timing controller, non-volatile memory and control interface.

117 **Type 2 Display Architecture:** One of the defined display module architectures. In DSI, DBI, DPI, and
118 DCS, a display module architecture in which a display module includes a display device, display driver IC,
119 partial-frame memory, registers, timing controller, non-volatile memory, control interface and video stream
120 interface.

121 **Type 3 Display Architecture:** One of the defined display module architectures. In DSI, DBI, DPI, and
122 DCS, a display module architecture in which a display module includes a display device, display driver IC,
123 registers, timing controller, non-volatile memory, control interface and video stream interface.

124 **Type 4 Display Architecture:** One of the defined display module architectures. In DSI, DBI, DPI, and
125 DCS, a display module architecture in which a display module includes a display device, display driver IC,
126 registers, timing controller, control lines and video stream interface.

127 2.2 Abbreviations

128 ↑ Rising edge active

129 ↓ Falling edge active

130	AGND	Power ground
131	CSX	Chip Select, active low
132	D/CX	Data/Command, Command is active low
133	DGND	Logic level ground
134	High-Z	High Impedance
135	H-Sync	Horizontal Synchronization
136	RESX	Reset signal, active low
137	RDX	Read signal
138	Ta	Ambient Temperature
139	WRX	Write signal
140	V _{DD}	Power Supply
141	V _{DDI}	Logic Level Supply
142	V-Sync	Vertical Synchronization

143 **2.3 Acronyms**

144	ASIC	Application Specific Integrated Circuit
145	CMOS	Complementary Metal Oxide Semiconductor
146	DBI	Display Bus Interface
147	DCS	Display Command Set
148	DOI	Dependent On Implementation
149	DSI	Display Serial Interface
150	I/O	Input/Output
151	LSB	Least Significant Bit
152	MIPI	Mobile Industry Processor Interface
153	MSB	Most Significant Bit

154 **3 References**

- 155 [1] MIPI Alliance Standard for Display Command Set, version 0.37, October 2005
- 156 [2] MIPI Alliance Standard for Display Parallel Interface, version 0.xx, August 2005
- 157 [3] MIPI Alliance Standard for Display Serial Interface, version 0.xx, August 2005

158 **4 Display Architectures and Interface Constructions**

159 **4.1 Display Architectures**

160 The display module shall be based on Type 1, Type 2, Type 3 or Type 4 display architecture.

161 The Type 1 Display Architecture should consist of the following functional blocks:

162 Display Device. Used to show the image data.

163 Display Driver. May be one or more devices used to drive the display device.

164 Full-frame memory. Used to hold the image data; can be integrated in the display driver.

165 Registers. Used to configure the display module behavior and hold identification information; can
166 be integrated in the display driver.

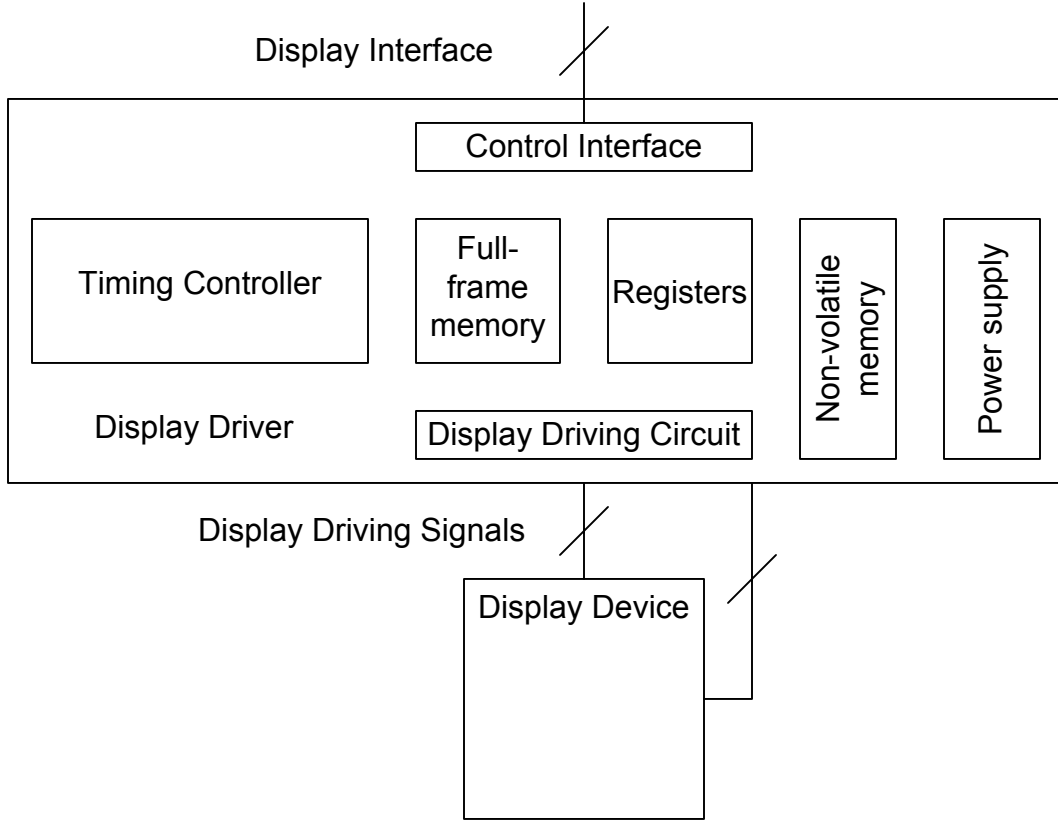
167 Timing Controller. Provides timing signals to control the display device and display driver based
168 on configuration information; can be integrated in the display driver.

169 Non-volatile memory. Used to store default register and configuration values; can be integrated in
170 the display driver.

171 Control Interface. Provides the interface between the host processor and the display driver; can be
172 integrated in the display driver.

173 Display Driving Circuit. As a part of display driver, used to convert timing signals and voltages to
174 signals appropriate to drive the display device.

175 Power Supply. Used to convert system voltages to levels usable by the display device and display
176 driver; can be integrated in the display driver.

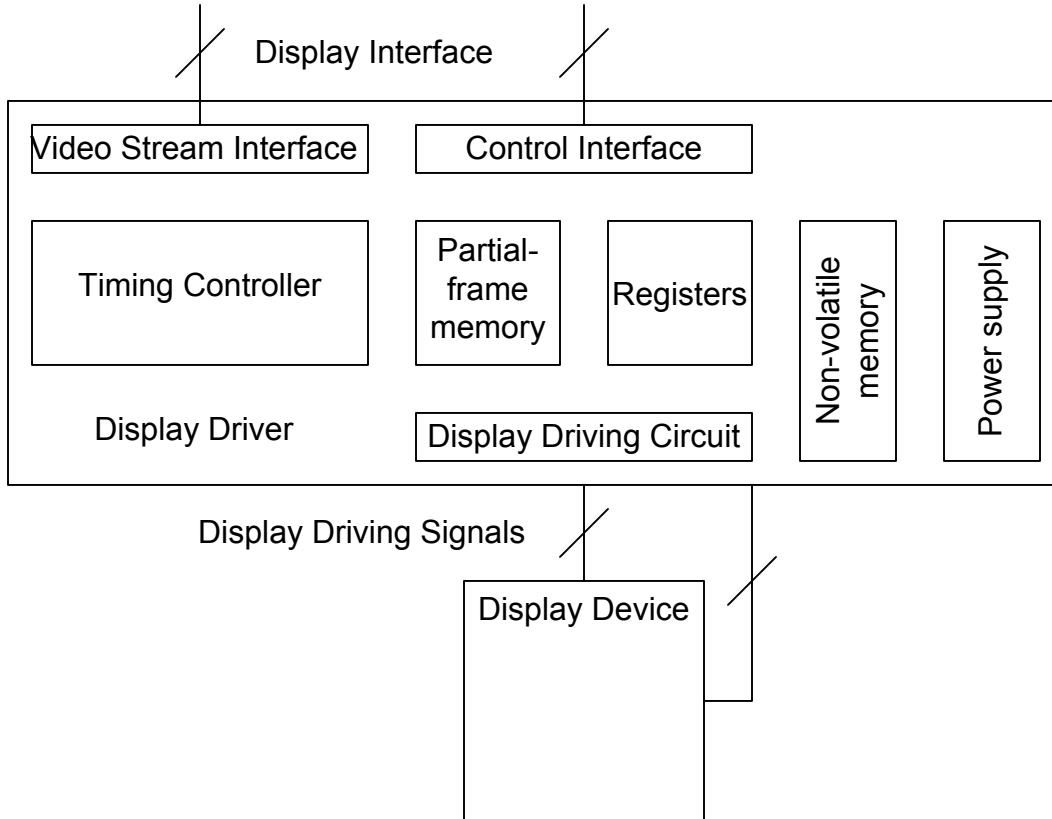


177

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Figure 1 Type 1 Display Architecture Block Diagram

- 179 The Type 2 Display Architecture should consist of the following functional blocks:
- 180 Display Device. Used to show image data.
- 181 Display Driver. May be one or more devices used to drive the display device.
- 182 Partial-frame memory. Used to hold image data. Can be integrated in the display driver.
- 183 Registers. Used to configure the display module behavior and hold identification information; can
184 be integrated in the display driver.
- 185 Timing Controller. Provides timing signals to control the display device and display driver based
186 on configuration information; can be integrated in the display driver.
- 187 Non-volatile memory. Used to store default register and configuration values; can be integrated in
188 the display driver.
- 189 Control Interface. Provides the interface between the host processor and the display driver; can be
190 integrated in the display driver.
- 191 Display Driving Circuit. As a part of display driver, used to convert timing signals and voltages to
192 signals appropriate to drive the display device.
- 193 Power Supply. Used to convert system voltages to levels usable by the display device and display
194 driver; can be integrated in the display driver.
- 195 Video Stream Interface. Used to receive video image data and timing signals from the host
196 processor.

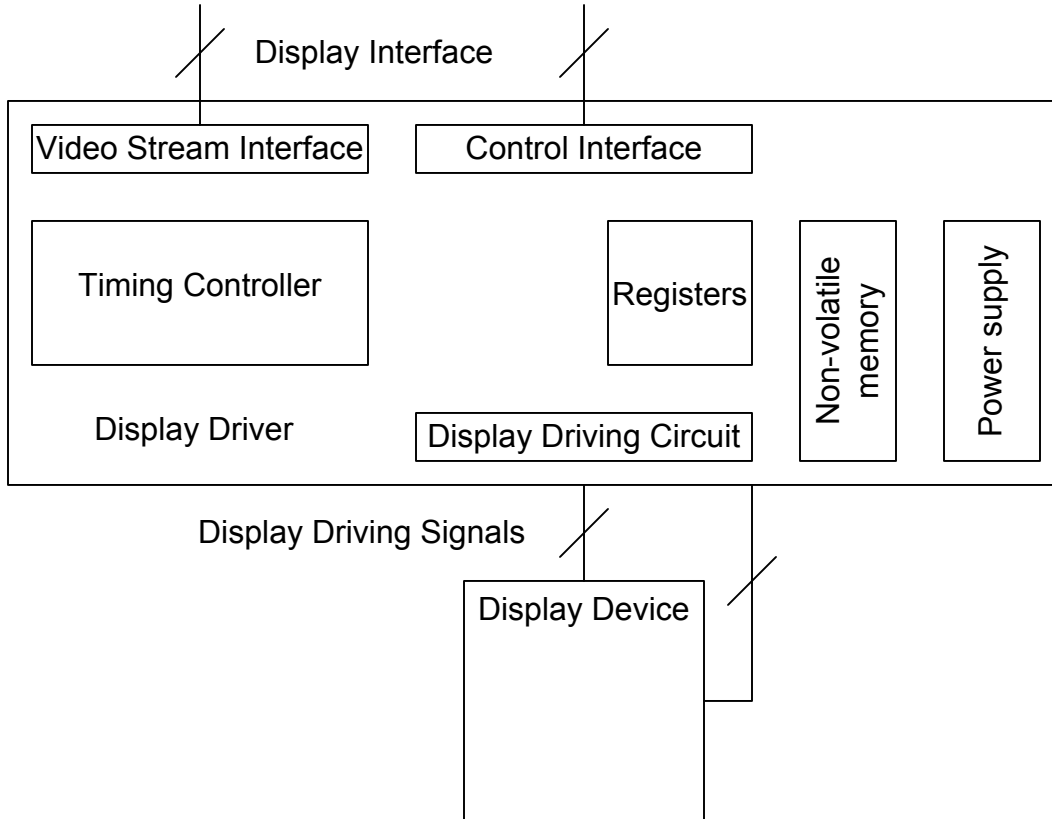


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198

Figure 2 Type 2 Display Architecture Block Diagram

- 199 The Type 3 Display Architecture should consist of the following functional blocks:
- 200 Display Device. Used to show image data.
- 201 Display Driver. May be one or more devices used to drive the display device.
- 202 Registers. Used to configure the display module behavior and hold identification information; can
203 be integrated in the display driver.
- 204 Timing Controller. Provides timing signals to control the display device and display driver based
205 on configuration information; can be integrated in the display driver.
- 206 Non-volatile memory. Used to store default register and configuration values; can be integrated in
207 the display driver.
- 208 Control Interface. Provides the interface between the host processor and the display driver; can be
209 integrated in the display driver.
- 210 Display Driving Circuit. As a part of display driver, used to convert timing signals and voltages to
211 signals appropriate to drive the display device.
- 212 Power Supply. Used to convert system voltages to levels usable by the display device and display
213 driver; can be integrated in the display driver.
- 214 Video Stream Interface. Used to receive video image data and timing signals from the host
215 processor.



216

217

Figure 3 Type 3 Display Architecture Block Diagram

218 The Type 4 Display Architecture should consist of the following functional blocks:

219 Display Device. Used to show image data.

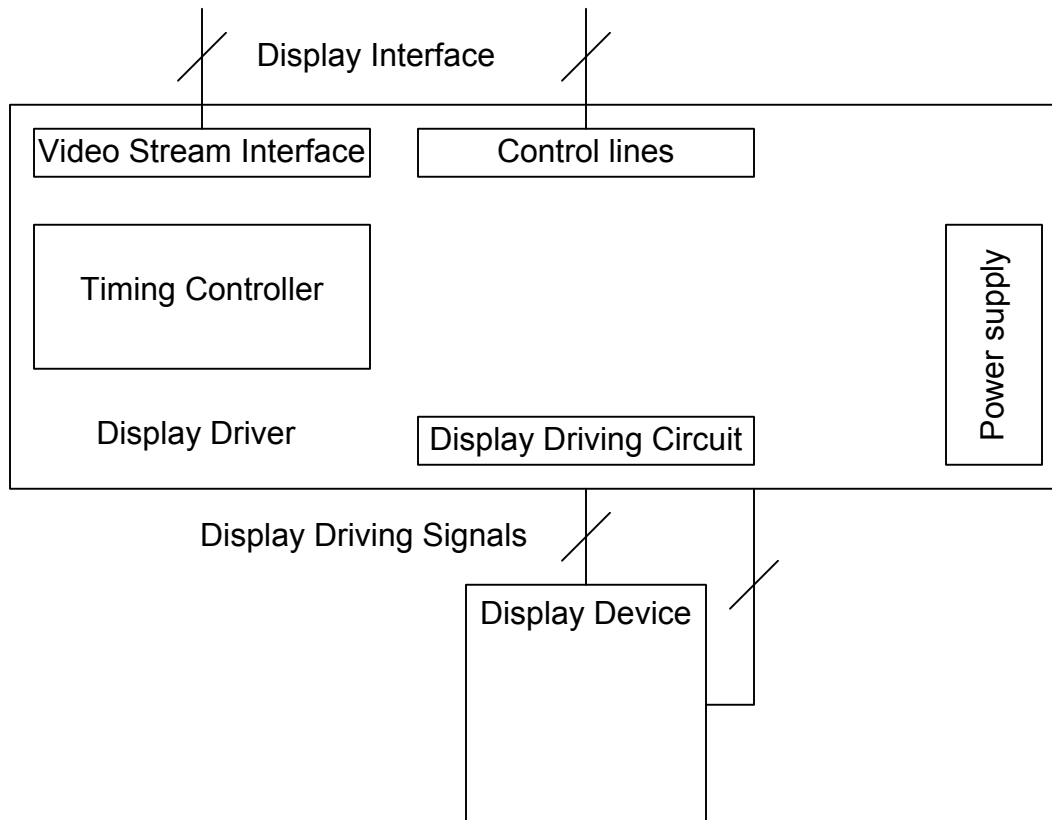
220 Display Driver. May be one or more devices used to drive the display device.

221 Timing Controller. Provides timing signals to control the display device and display driver based
222 on configuration information; can be integrated in the display driver.

223 Control lines. Used to receive display behavior control information from the host processor.

224 Display Driving Circuit. As a part of display driver, used to convert timing signals and voltages to
225 signals appropriate to drive the display device.

226 Power Supply. Used to convert system voltages to levels usable by the display device and display
227 driver; can be integrated in the display driver.



228

229

Figure 4 Type 4 Display Architecture Block Diagram

230 In all architecture types, it is assumed the power supply is under the control of the display driver.

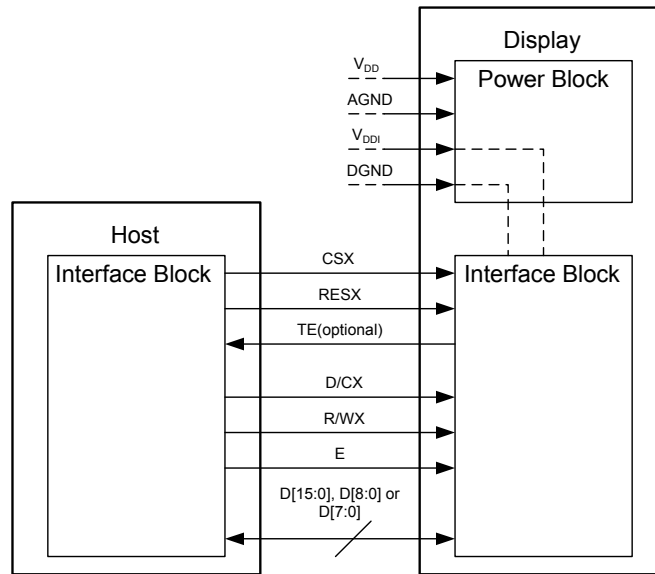
231 DBI is used for the control interfaces.

232 Refer to *MIPI Alliance Standard for Display Parallel Interface* [2] for the video stream interface used in
233 type 2, 3 and 4 architectures.

234 **4.2 Display Bus Interface Constructions**

235 The electrical connection between the host processor and a display module consists of two blocks: power
 236 and interface. Power is supplied from either the host processor itself or another device under the control of
 237 the host to the power block of the display module. Interface blocks are used to transfer information
 238 between the host processor and a display module.

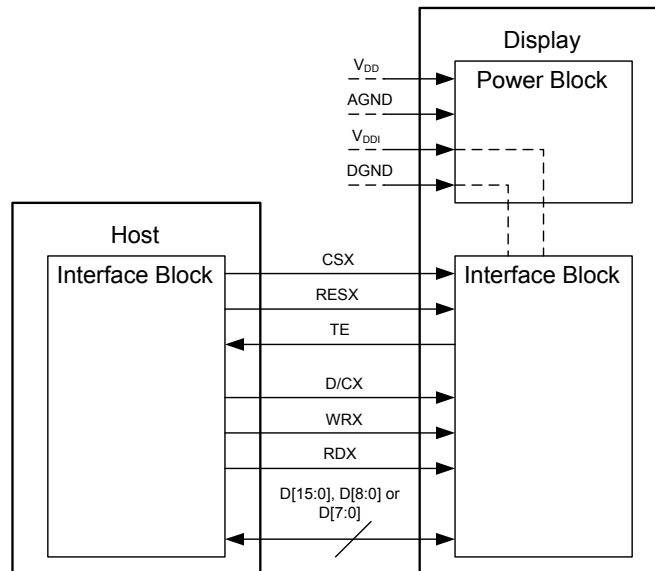
239 There are three types of DBI implementations, named type A, B and C as shown in Figure 5, Figure 6 and
 240 Figure 7, respectively.



241

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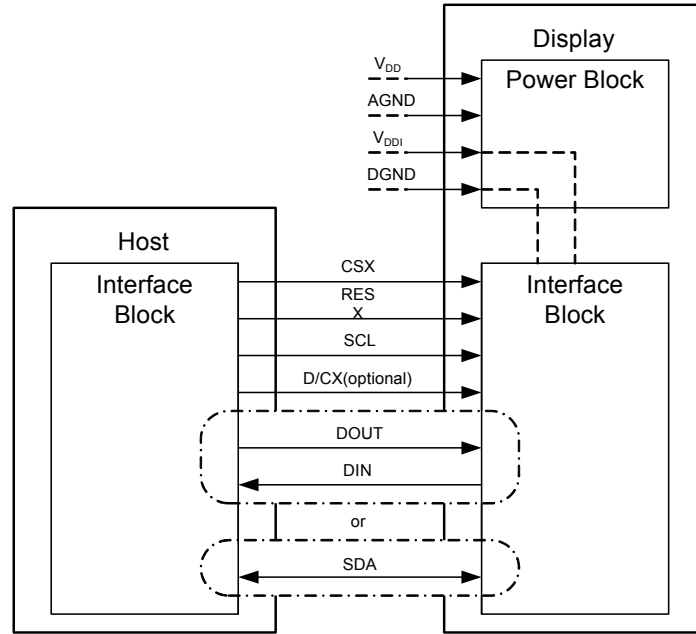
Figure 5 Type A Interface Block Diagram



243

244

Figure 6 Type B Interface Block Diagram



245
246

Figure 7 Type C Interface Block Diagram

247 **5 Interface Signal Description**248 **5.1 Power Supply Signals**249 **Table 1 Power Supply Signals**

Symbol	Name	Description
V _{DD}	Power supply	Power supply for display module
V _{DDI}	Logic level supply	Logic level supply for interface signals
AGND	Power Ground	GND for power supply
DGND	Logic level ground	GND for logic level

250 **5.2 Interface Signals**251 **5.2.1 Type A Interface**252 **Table 2 Type A Interface Signal Description**

Symbol	Name	I/O	Description
CSX	Chip Select	O	In Fixed E mode, host processor writes data (D[15:0], D[8:0] or D[7:0]) at falling edge, or reads at rising edge. In Clocked E mode, the display module is selected when low.
R/WX	Read/Write	O	Host processor reads data (D[15:0], D[8:0] or D[7:0]) when high or writes data (D[15:0], D[8:0] or D[7:0]) when low.
E	E clock	O	In Fixed E mode, this signal is tied high. In Clocked E mode, the host processor reads information (D[15:0], D[8:0], D[7:0]) at rising edge or writes at falling edge.
D[15:0], D[8:0], or D[7:0]	Information	I/O	Information signals
D/CX	Data/Command	O	Data is indicated when high and Command is indicated when low.
RESX	Reset	O	Display module is reset when low.
TE	Tearing Effect	I	Tearing Effect (optional).

253 Note: I/O directions are defined from the host processor perspective.

254 When CSX is high, the display module ignores all other interface signals.

255 CSX can be connected to DGND permanently on the display module without limitations.

256 5.2.2 Type B Interface

257 **Table 3 Type B Interface Signal Description**

Symbol	Name	I/O	Description
CSX	Chip Select	O	Display module is selected when low.
RDX	Read	O	Host processor reads information (D[15:0], D[8:0] or D[7:0]) at rising edge.
WRX	Write	O	Host processor writes information (D[15:0], D[8:0] or D[7:0]) at falling edge.
D[15:0], D[8:0] or D[7:0]	Information	I/O	Information signals
D/CX	Data/Command	O	Data is indicated when high and Command is indicated when low.
RESX	Reset	O	Display module is reset when low.
TE	Tearing Effect	I	Tearing Effect

258 Notes:

259 I/O directions are defined from the host processor perspective.

260 When CSX is high, the display module ignores all other interface signals.

261 CSX can be connected to DGND permanently on the display module without limitations.

262 5.2.3 Type C Interface

263 **Table 4 Type C Interface Signal Description**

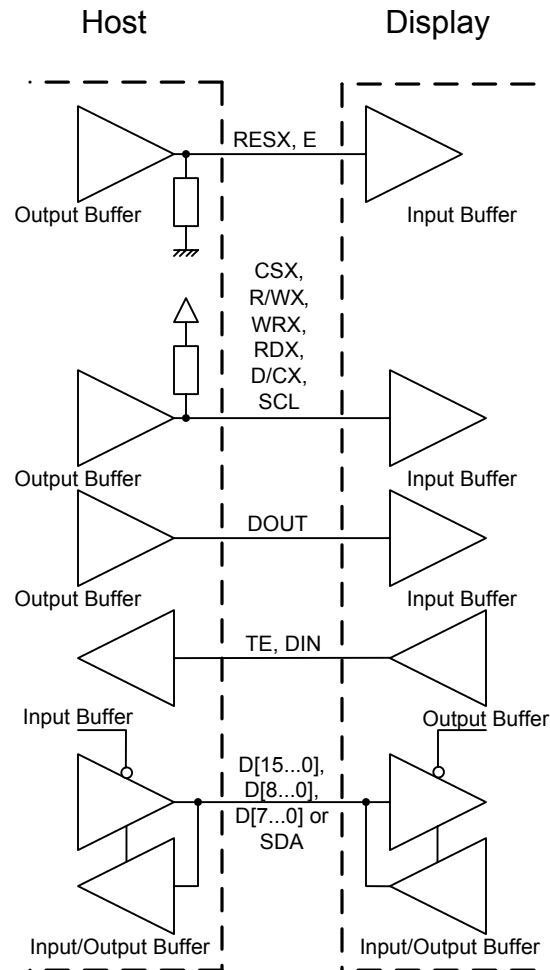
Symbol	Name	I/O	Description
CSX	Chip Select	O	Display is selected when low.
SCL	Serial Clock	O	Host processor writes information (DOUT or SDA) or reads information (DIN or SDA) at rising edge
DOUT	Information Out	O	Information signal output from host processor
DIN	Information In	I	Information signal input to host processor
SDA	Information	I/O	Bidirectional information signal

Symbol	Name	I/O	Description
D/CX	Data/Command	O	Data is indicated when high and Command is indicated when low (optional).
RESX	Reset	O	Display is reset when low.

- 264 Notes:
- 265 I/O directions are defined from the host perspective.
- 266 When CSX is high, display module ignores all other interface signals.
- 267 CSX can be connected to DGND permanently on the display without limitations.

268 **6 Interface I/O Cells**

269 The host processor and display module interface blocks shall be implemented using CMOS I/O cells for
 270 interface signals as they are described in Figure 8.



271
 272 **Figure 8 Interface I/O Cells**

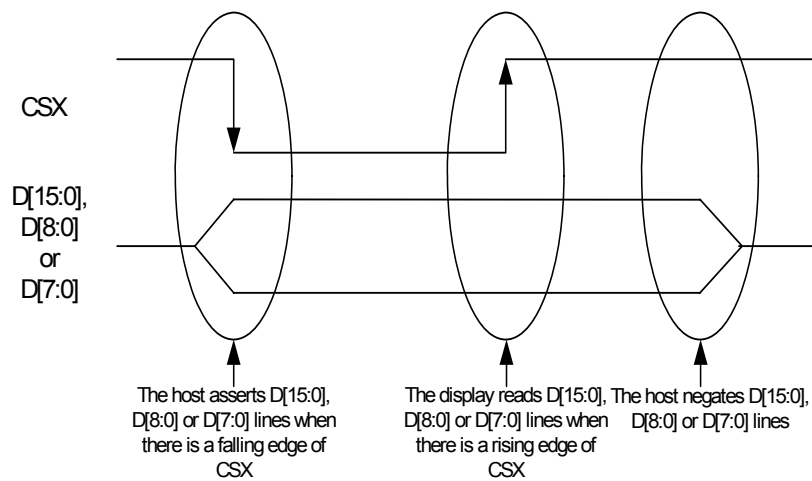
273 7 Interface Functional Description

274 7.1 Type A Interface Write and Read Cycles

275 7.1.1 Write Cycle

276 During a write cycle the host processor writes commands or data to the display module via the interface.
 277 Type A interfaces support two modes: Fixed E and Clocked E. Both modes utilize CSX, D/CX, R/WX and
 278 E signals as well as all eight (D[7:0]), nine (D[8:0]) or sixteen (D[15:0]) information signals. D/CX is
 279 driven low while a command is present on the interface and pulled high when data is on the interface.

280 The write cycle is described in Figure 9 and Figure 10.



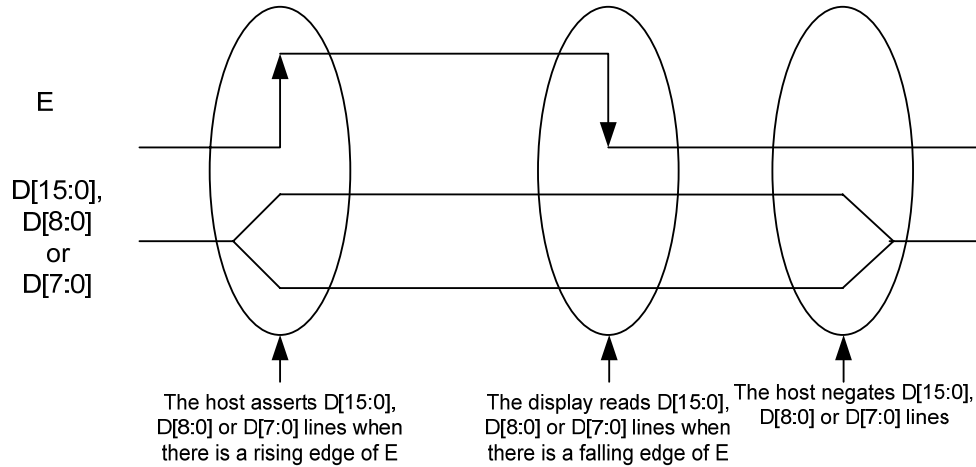
281

282

Figure 9 Type A Interface - Fixed E Mode Write Cycle

283 Note:

- 284 1. CSX is an unsynchronized signal; it can be stopped.
 285 2. E signal is tied high in Fixed E mode.



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287

Figure 10 Type A Interface - Clocked E Mode Write Cycle

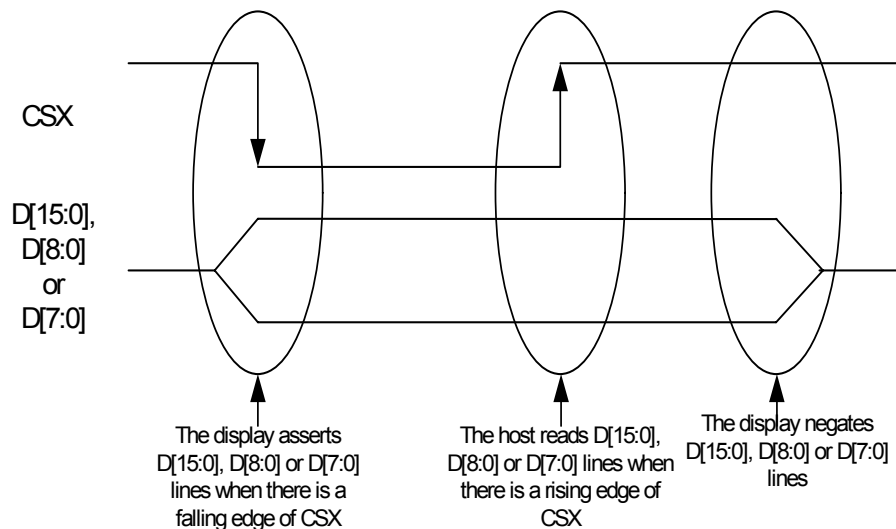
288 Notes:

- 289 1. E is an unsynchronized signal; it can be stopped.
- 290 2. CSX is asserted (taken low) for the same duration as the information signals.

291 **7.1.2 Read Cycle**

292 During a read cycle the host processor reads data from the display module via the interface. Type A
 293 interfaces support two modes: Fixed E and Clocked E. Both modes utilize CSX, D/CX, R/WX and E
 294 signals as well as all eight (D[7:0]), nine (D[8:0]) or sixteen (D[15:0]) information signals. D/CX is driven
 295 low during the entire read cycle.

296 The read cycle is described in Figure 11 and Figure 12.



297

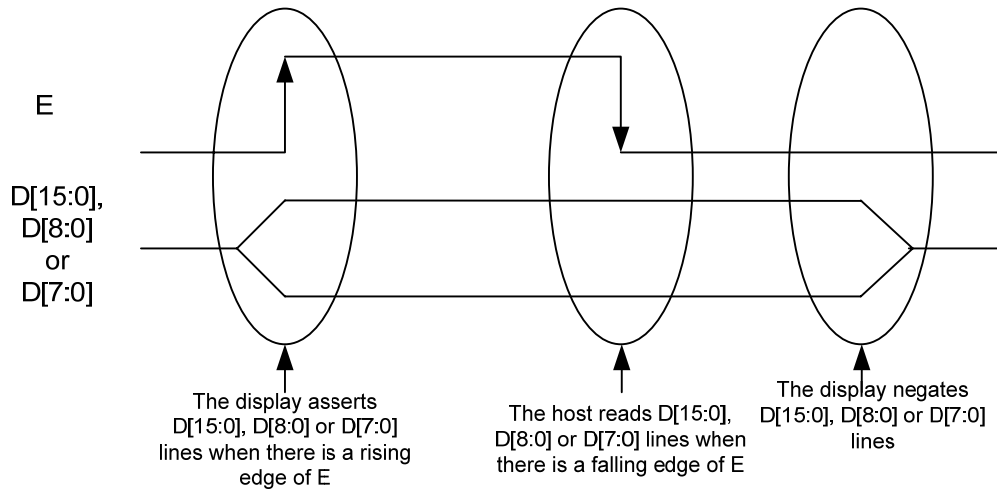
298

Figure 11 Type A Interface - Fixed E Mode Read Cycle

299 Note:

- 300 1. CSX is an unsynchronized signal; it can be stopped.

- 301 2. E signal is tied up to high in Fixed E mode.
 302



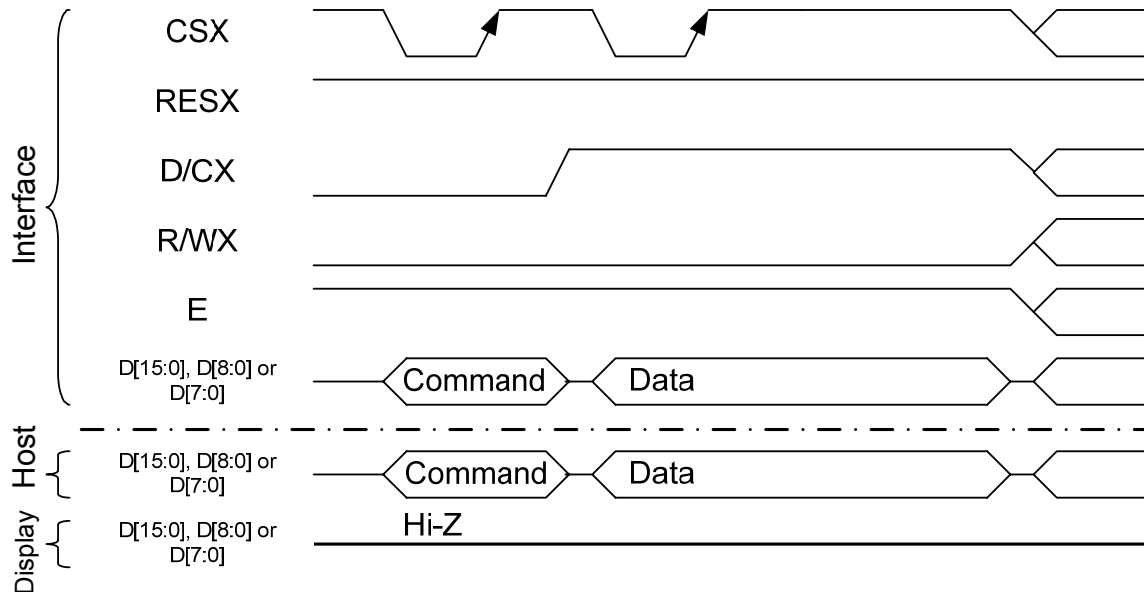
303
 304

Figure 12 Type A Interface - Clocked E Mode Read Cycle

305 Note:

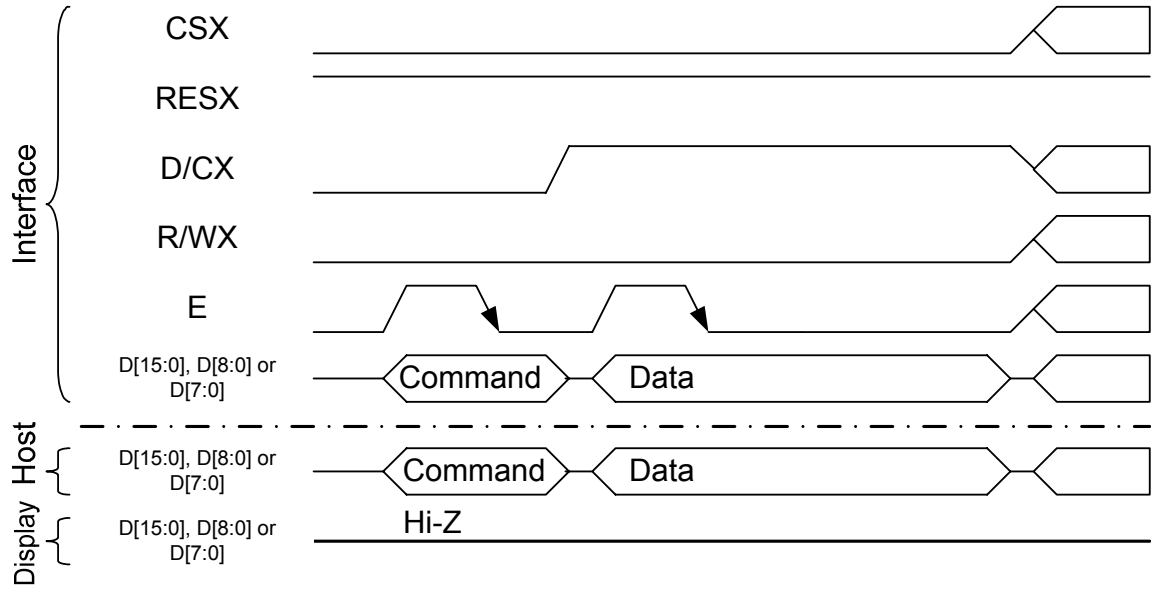
- 306 1. E is an unsynchronized signal; it can be stopped.
 307 2. CSX is asserted (taken low) for the same duration as the information signals.

308 **7.1.3 Display Read/Write Sequences**



309
 310

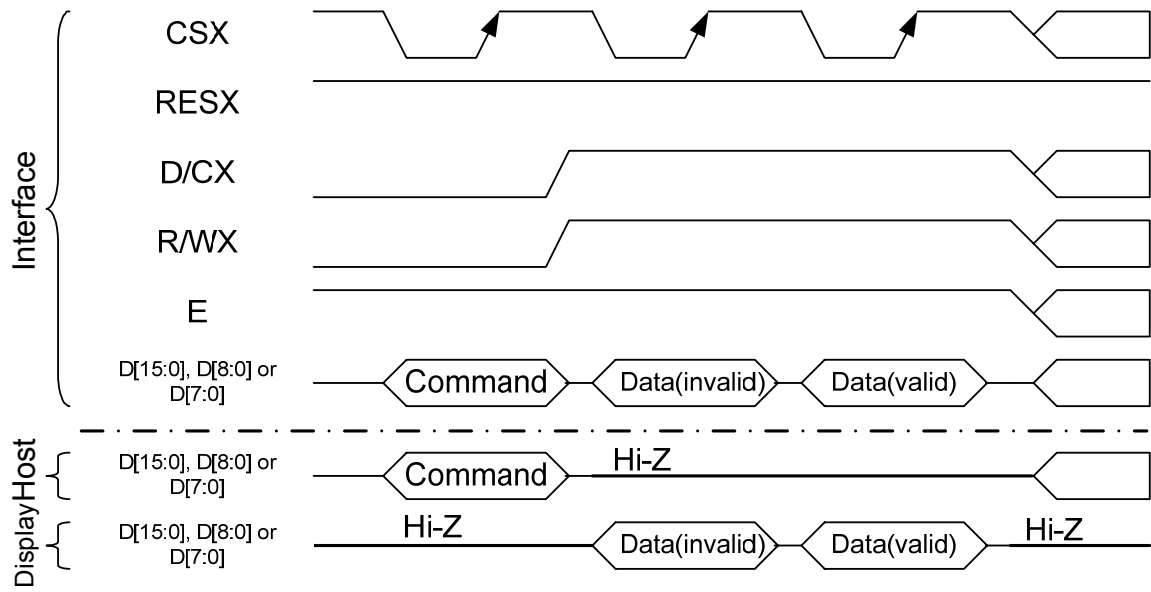
Figure 13 Type A Interface - Example Fixed E Mode Write Sequence



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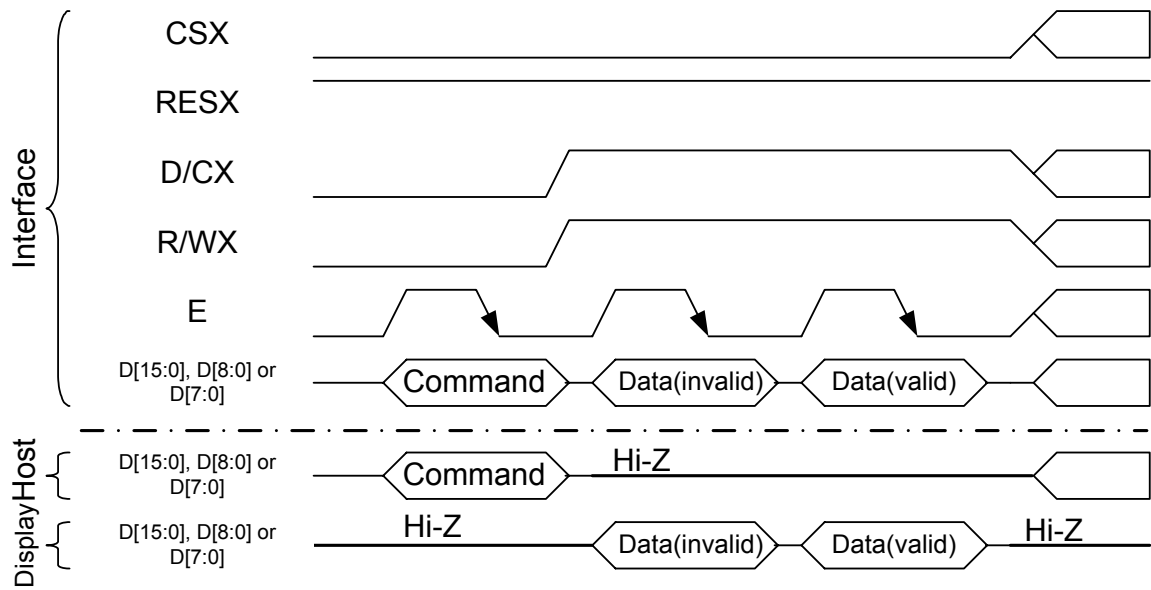
Figure 14 Type A Interface - Example Clocked E Mode Write Sequence



313

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Figure 15 Type A Interface - Example Fixed E Mode Read Sequence



315

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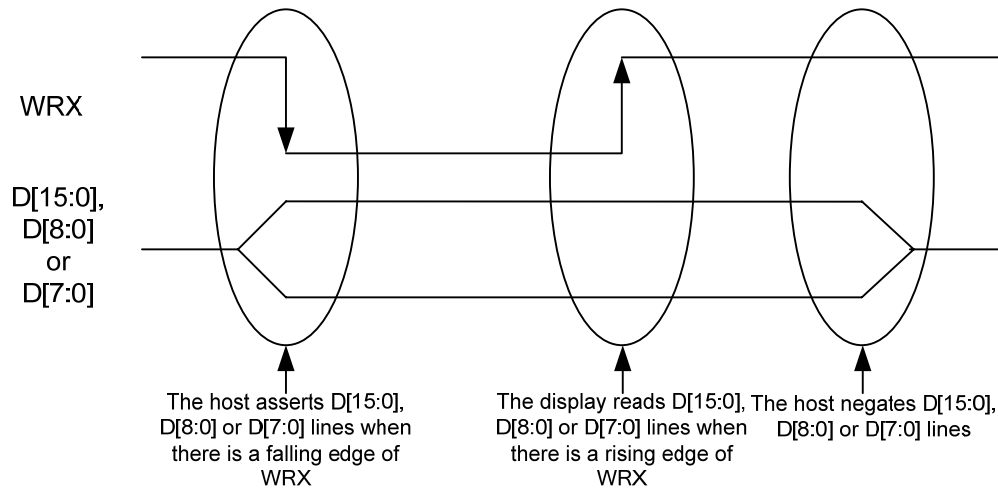
Figure 16 Type A Interface - Example Clocked E Mode Read Sequence

317 7.2 Type B Interface Write and Read Cycles

318 7.2.1 Write Cycle

319 During a write cycle the host processor sends data to the display module via the interface. The Type B
 320 interface utilizes D/CX, RDX and WRX signals as well as all eight (D[7:0]), nine (D[8:0]) or sixteen
 321 (D[15:0]) information signals. WRX is driven from high to low then pulled back to high during the write
 322 cycle. The host processor provides information during the write cycle while the display module reads the
 323 host processor information on the rising edge of WRX. D/CX is driven low while command information is
 324 on the interface and is pulled high when data is present.

325 Figure 17 shows a write cycle for the type B interface.



326

327

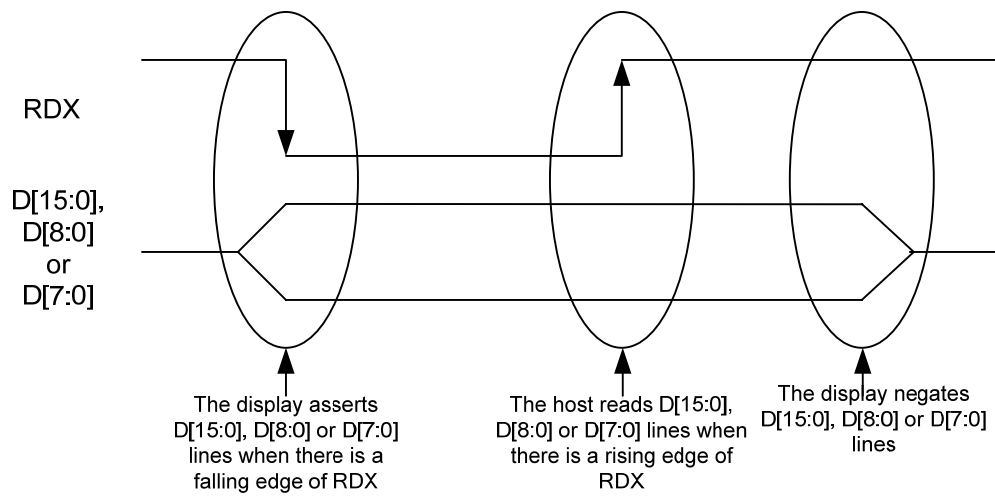
Figure 17 Type B Interface - Write Cycle

328 Note: WRX is an unsynchronized signal; it can be stopped.

329 7.2.2 Read Cycle

330 During a read cycle the host processor reads data from the display module via the interface. The Type B
 331 interface utilizes D/CX, RDX and WRX signals as well as all eight (D[7:0]), nine (D[8:0]) or sixteen
 332 (D[15:0]) information signals. RDX is driven from high to low then allowed to be pulled back to high
 333 during the read cycle. The display module provides information to the host processor during the read cycle
 334 while the host processor reads the display module information on the rising edge of RDX. D/CX is driven
 335 high during the read cycle.

336 Figure 18 shows the read cycle for the type B interface.



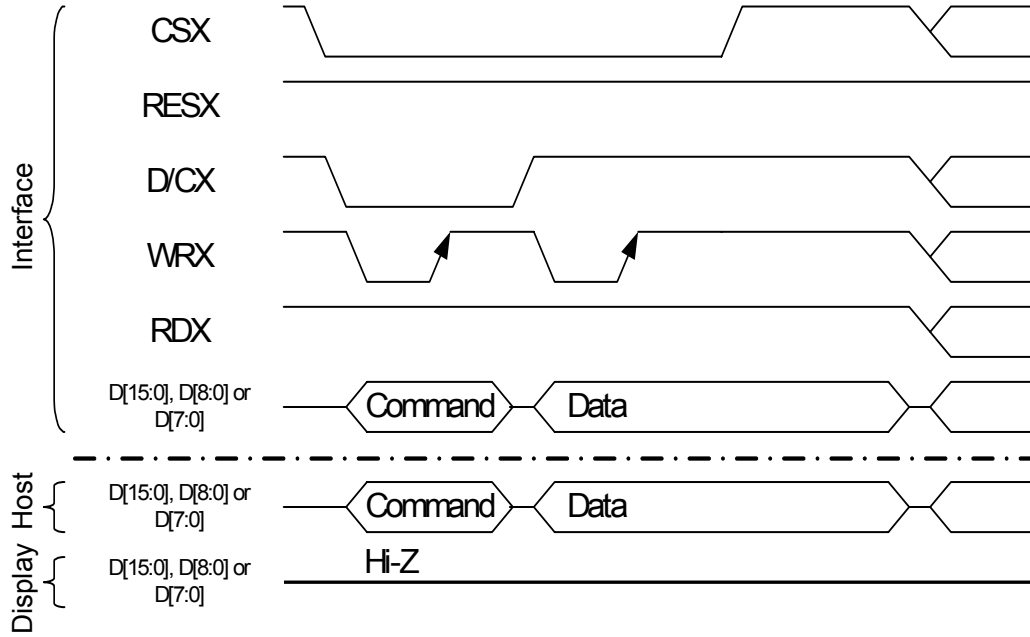
337

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Figure 18 Type B Interface - Read Cycle

339 Note: RDX is an unsynchronized signal; it can be stopped.

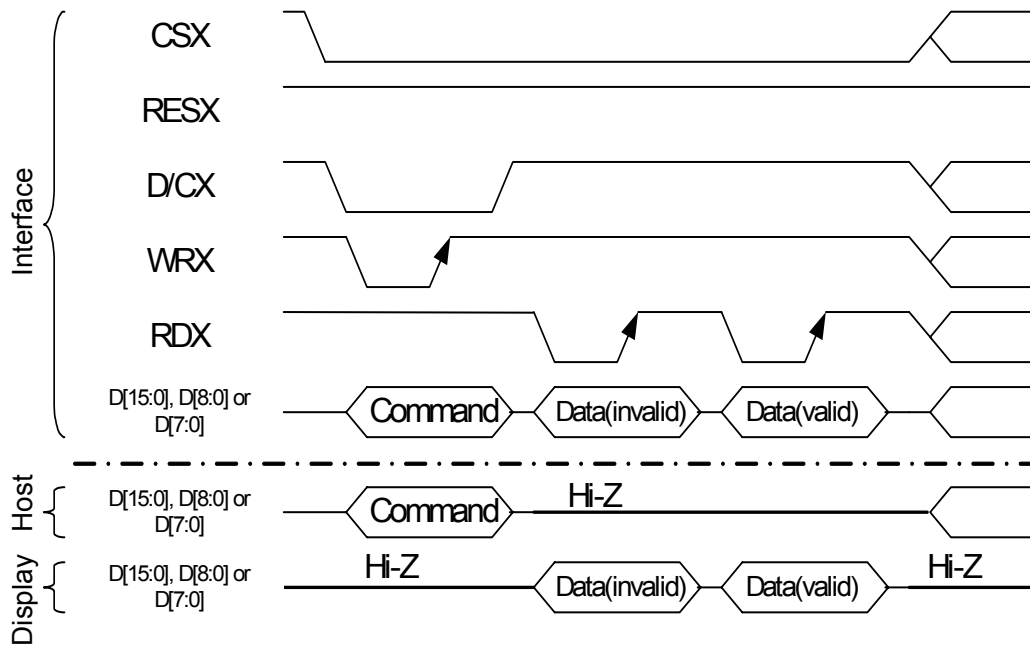
340 **7.2.3 Display Read/Write Sequences**



341

342

Figure 19 Type B Interface Write Sequence



343

344

Figure 20 Type B Interface Read Sequence

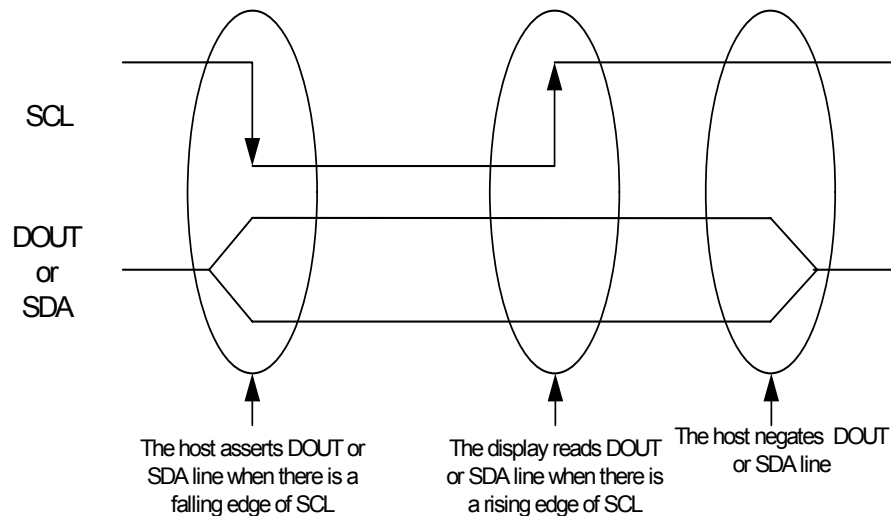
345 Note: Read Data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then
 346 the display information outputs will be High-Z.

347 7.3 Type C Interface Write and Read Sequences

348 7.3.1 Write Cycle and Sequence

349 During a write cycle the host processor sends a single bit of data to the display module via the interface.
 350 The Type C interface utilizes CSX, SCL and SDA or DOUT signals. SCL is driven from high to low then
 351 pulled back to high during the write cycle. The host processor provides information during the write cycle
 352 while the display module reads the host processor information on the rising edge of SCL.

353 Figure 21 shows the write cycle for the type C interface.



354

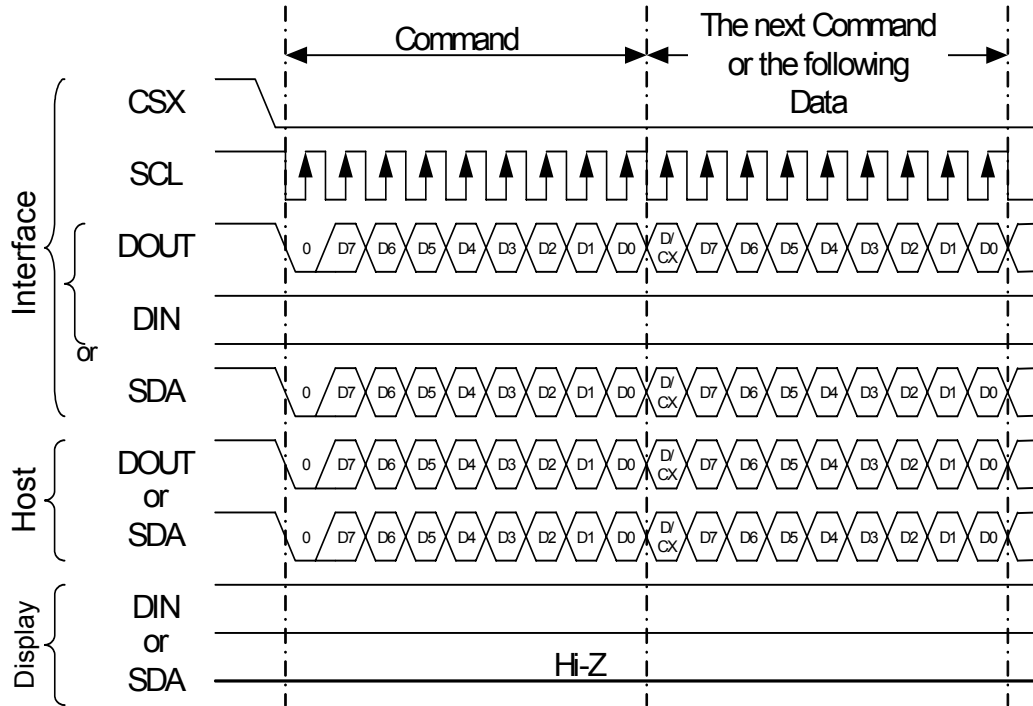
355

Figure 21 Type C Interface Write Cycle

356 Note: SCL is an unsynchronized signal; it can be stopped.

357 During the write sequence the host processor writes one or more bytes of information to the display
 358 module via the interface. The write sequence is initiated when CSX is driven from high to low and ends
 359 when CSX is pulled high. Each byte is either nine or sixteen write cycles in length. If the optional D/CX
 360 signal is used a byte is eight write cycles long. D/CX is driven low while command information is on the
 361 interface and is pulled high when data is present.

362 The type C interface write sequences are described in Figure 22, Figure 23 and Figure 24.

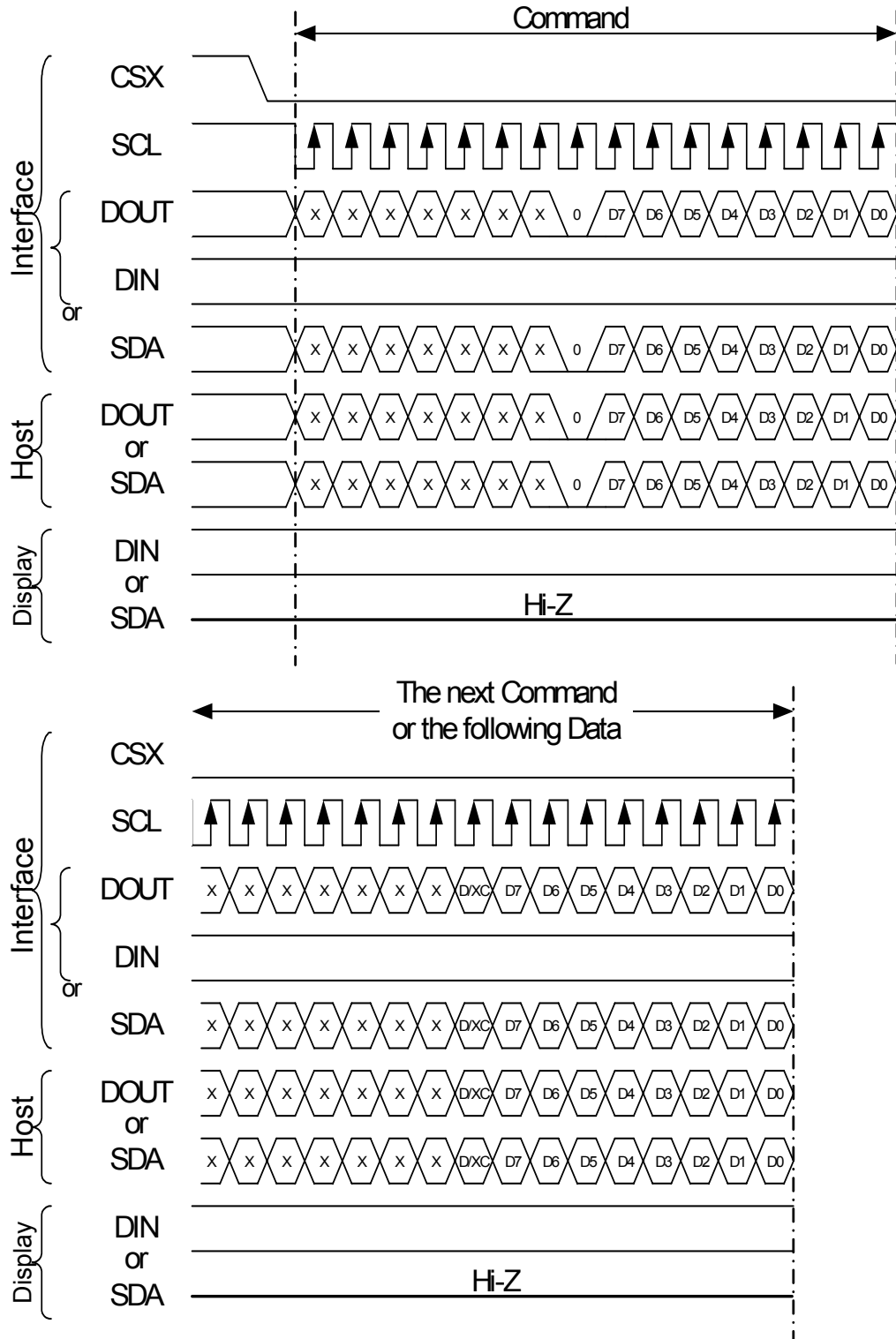


363

364

Figure 22 Type C Interface Write Sequence - Option 1

365 Note: D7 is MSB and D0 is LSB of byte.

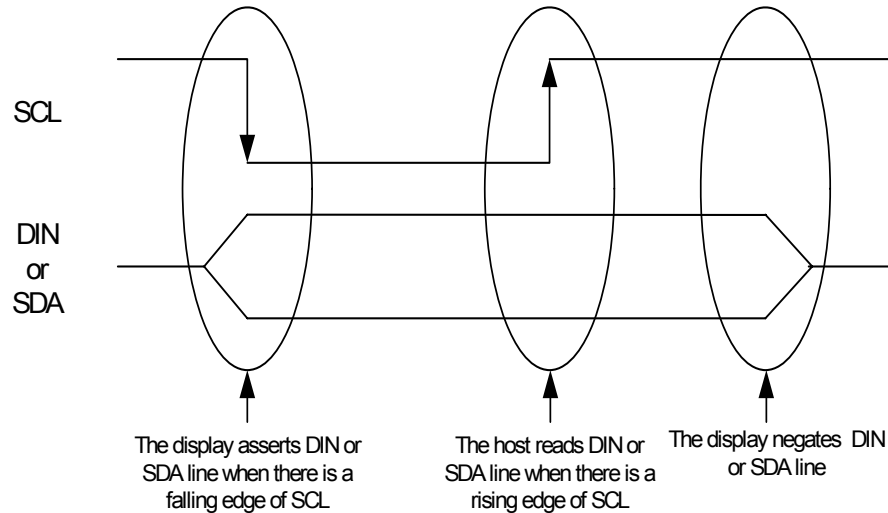


366

367

Figure 23 Type C Interface Write Sequence – Option 2

368 Note: D7 is MSB and D0 is LSB of byte.



379

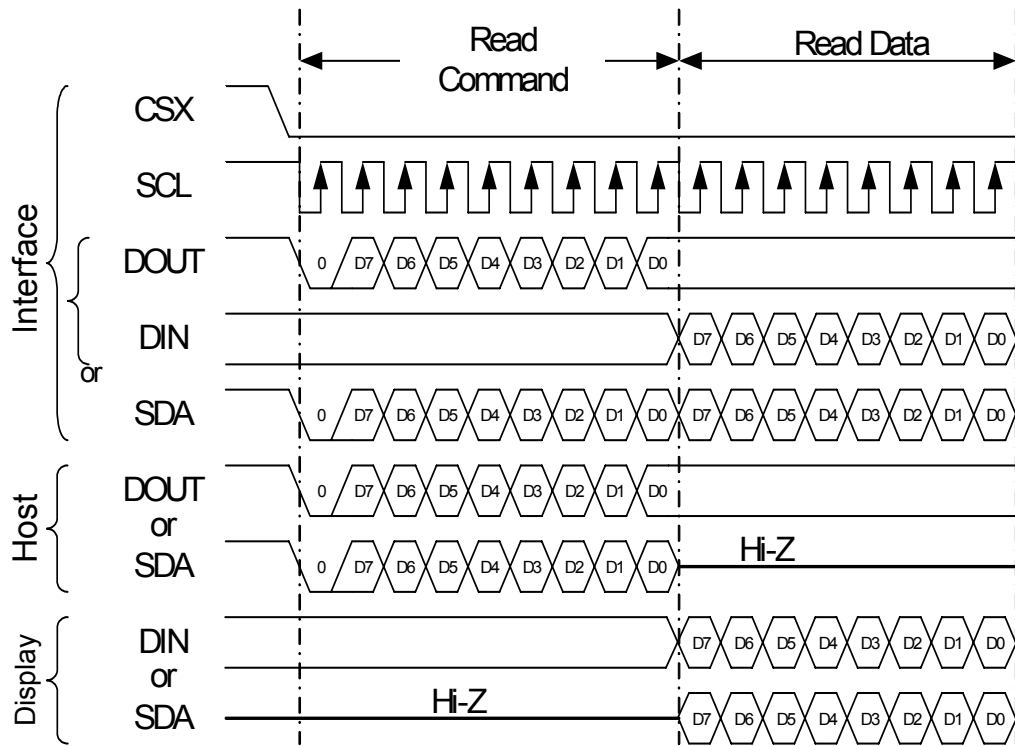
380

Figure 25 Type C Interface Read Cycle

381 Note: SCL is an unsynchronized signal; it can be stopped.

382 During the read sequence the host processor reads one or more bytes of information from the display
 383 module via the interface. The read sequence is initiated when CSX is driven from high to low and ends
 384 when CSX is pulled high. Each byte is either nine or sixteen write cycles in length. If the optional D/CX
 385 signal is used a byte is eight read cycles long. D/CX is driven low while command information is on the
 386 interface and is pulled high when data is present.

387 The type C interface read sequences are shown in Figure 26, Figure 27 and Figure 28.

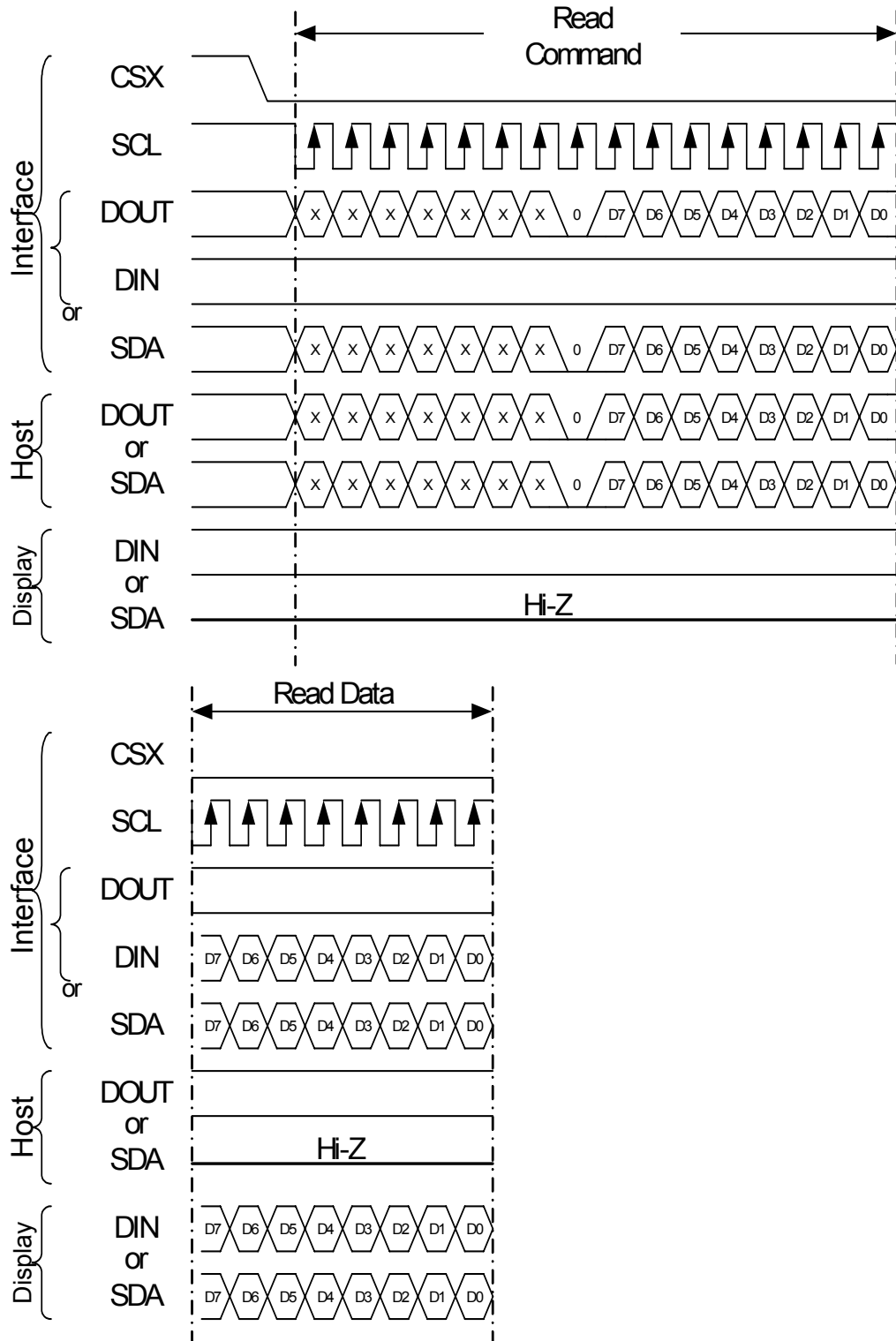


388

389

Figure 26 Type C Interface Read Sequence – Option 1

390 Note: D7 is MSB and D0 is LSB of byte.



391
392

Figure 27 Type C Interface Read Sequence – Option 2

393 Note: D7 is MSB and D0 is LSB of byte.

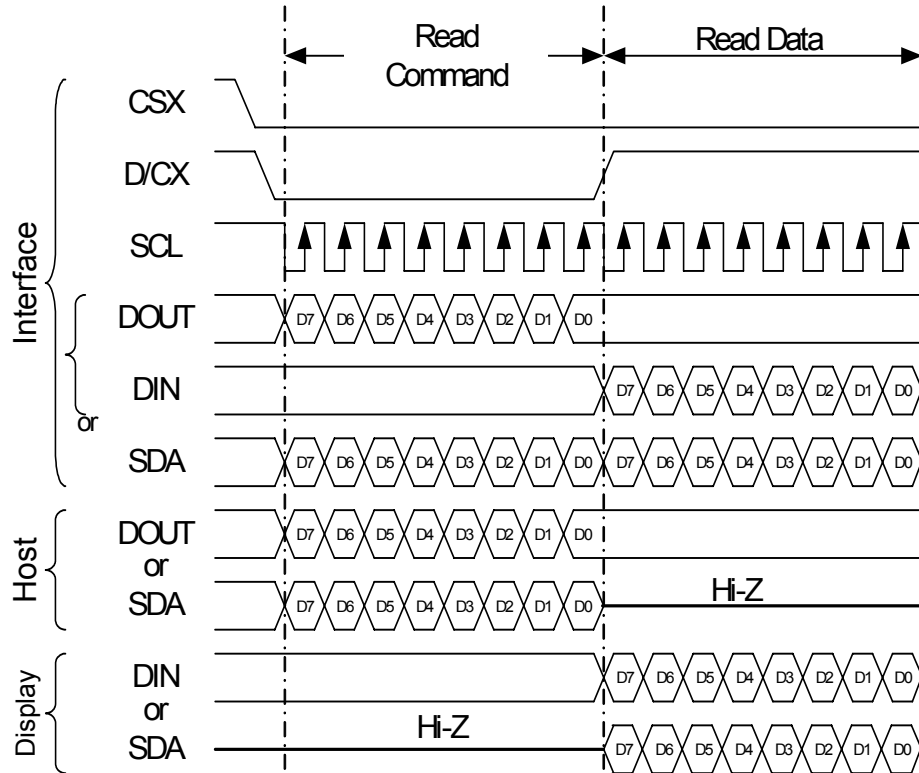


Figure 28 Type C Interface Read Sequence – Option 3

394
395

396 Note: D7 is MSB and D0 is LSB of byte.

397 **7.3.3 Break and Pause of Sequences**

398 The host processor can break a read or write sequence by pulling the CSX signal high during a command
399 or data byte. The display module shall reset its interface so it will be ready to receive the same byte when
400 CSX is again driven low.

401 The host processor can pause a read or write sequence by pulling the CSX signal high between command
402 or data bytes. The display module shall wait for the host processor to drive CSX low before continuing the
403 read or write sequence at the point where the sequence was paused.

404 **7.4 Tearing Effect**

405 The display module can use the Tearing Effect signal to provide the host processor with internal signal
406 information such as VSYNC as shown in Figure 29 or VSYNC + HSYNC as shown in Figure 30.



Figure 29 Tearing Effect Signal with VSYNC



Figure 30 Tearing Effect Signal with VSYNC + HSYNC

407
408

409
410

411 **8 Interface Electrical Characteristics**412 **8.1 Electrical Characteristics**413 **8.1.1 Absolute Maximum Ratings**414 **Table 5 Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
Power Supply	V_{DD}	DOI	V
Logic level supply	V_{DDI}	DOI	V
Logic Signal Input Voltage	V_I	DOI	V
Logic Signal Output Voltage	V_O	DOI	V

415 **8.1.2 DC Characteristics**416 **Table 6 DC Characteristics**

Parameter	Symbol	Condition	Specification			Unit
			min	typ	max	
Power Supply Voltage	V_{DD}	Operating Voltage		DOI		V
Logic High level input voltage	V_{IH}		$0.7V_{DDI}$		V_{DDI}	V
Logic Low level input voltage	V_{IL}		0.0		$0.3V_{DDI}$	V
Logic High level output voltage	V_{OH}	$I_{OUT} = -1 \text{ mA}$	$0.8V_{DDI}$		V_{DDI}	V
Logic Low level output voltage	V_{OL}	$I_{OUT} = +1 \text{ mA}$	0.0		$0.2V_{DDI}$	V
Logic High level input current	I_{IH}	Except D[15:0], D[8:0] or D[7:0]			10	uA
	I_{IHD}	D[15:0], D[8:0] or D[7:0]			10	uA
Logic Low level input current	I_{IL}	Except D[15:0], D[8:0] or D[7:0]	-10			uA
	I_{ILD}	D[15:0], D[8:0] or D[7:0]	-10			uA

417 Note: $T_a = -30$ to $70 \text{ }^\circ\text{C}$

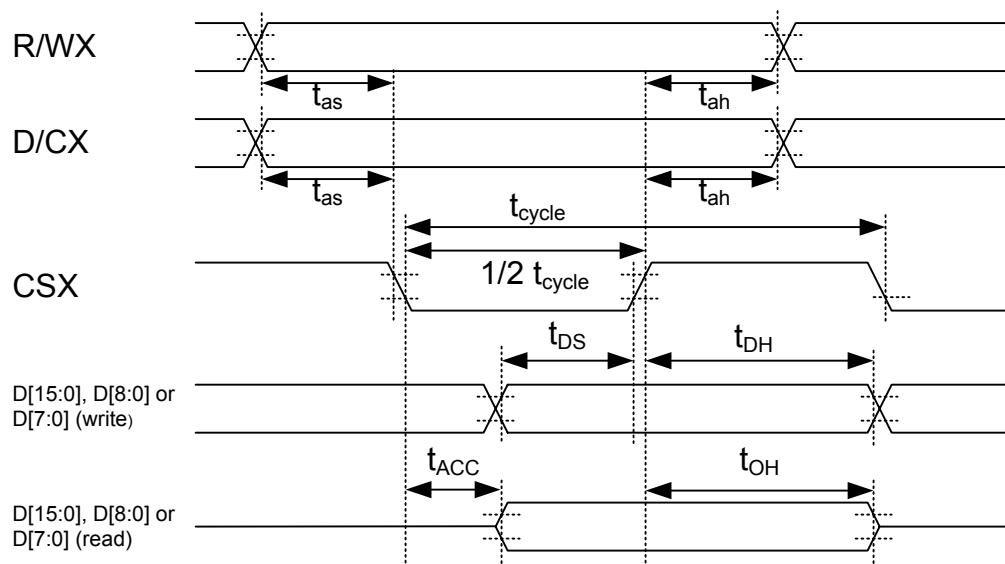
418

Table 7 Logic High level input voltage classification

Parameter	Symbol	Class	Specification			unit
			min	typ	max	
Logic High level input voltage	V_{DDI}	1	1.1	1.2	1.3	V
		2	1.4	1.5	1.6	V
		3	1.7	1.8	1.9	V
		4	2.6	2.8	3.0	V

419 Note: $T_a = -30$ to 70 °C

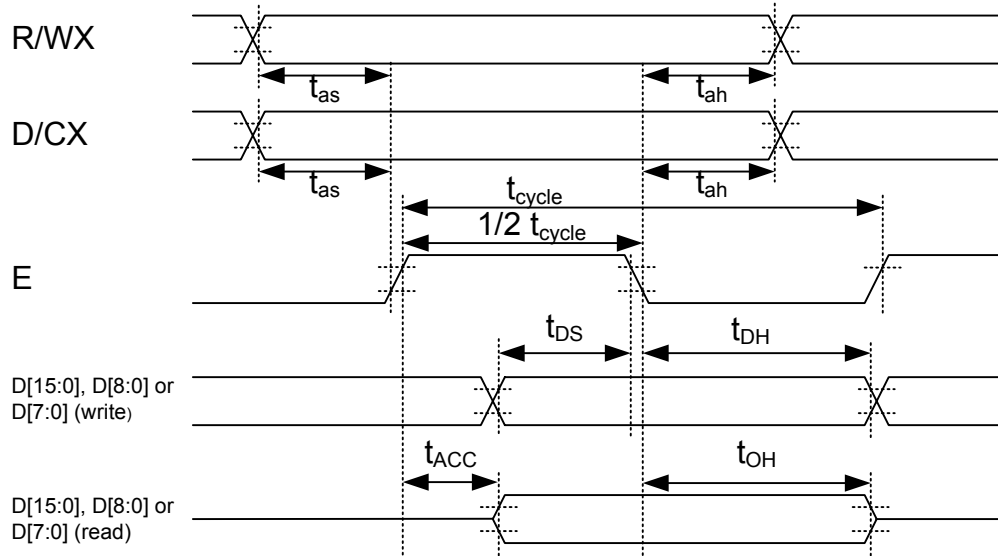
420 **8.1.3 AC Characteristics**



421

422

Figure 31 AC Characteristics, Type A Interface, Fixed E Mode



423

424

Figure 32 AC Characteristics, Type A Interface, Clocked E Mode

425

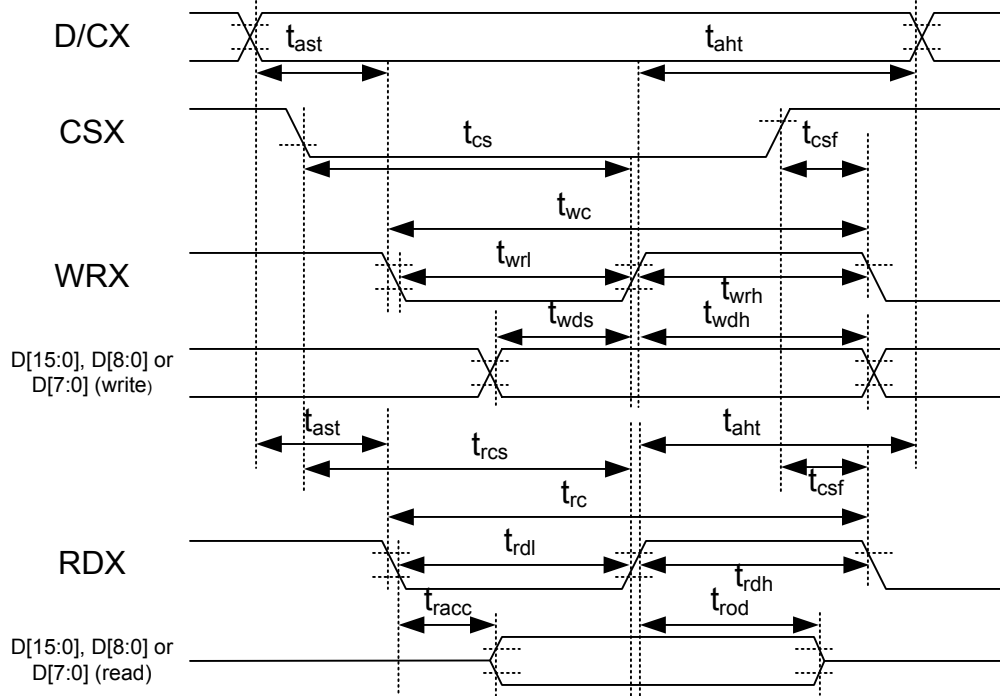
Table 8 AC Characteristic -- Type A Interface

Signal	Symbol	Parameter	min	max	Unit	Description
R/WX or D/CX	t_{as}	Address setup time	T	-	ns	
	t_{ah}	Address hold time (Write/Read)	T	-	ns	
CSX or E	t_{cycle}	System clock cycle time	5xT	79xT	ns	
D[15:0], D[8:0], or D[7:0]	t_{DS}	Data setup time	15	-	ns	For maximum $C_L=30pF$
	t_{DH}	Data hold time	25		ns	
	t_{ACC}	Data access time	10		ns	For minimum $C_L=8pF$
	t_{OH}	Output hold time	10		ns	

426 Note:

427 1. $T_a = -30$ to 70 °C, V_{DDI} range: according to Logic High level input voltage classification, GND =
428 0V, $T = 10 \pm 0.5$ ns

429 2. Does not include signal rise and fall times.



430

431

Figure 33 AC Characteristics, Type B Interface

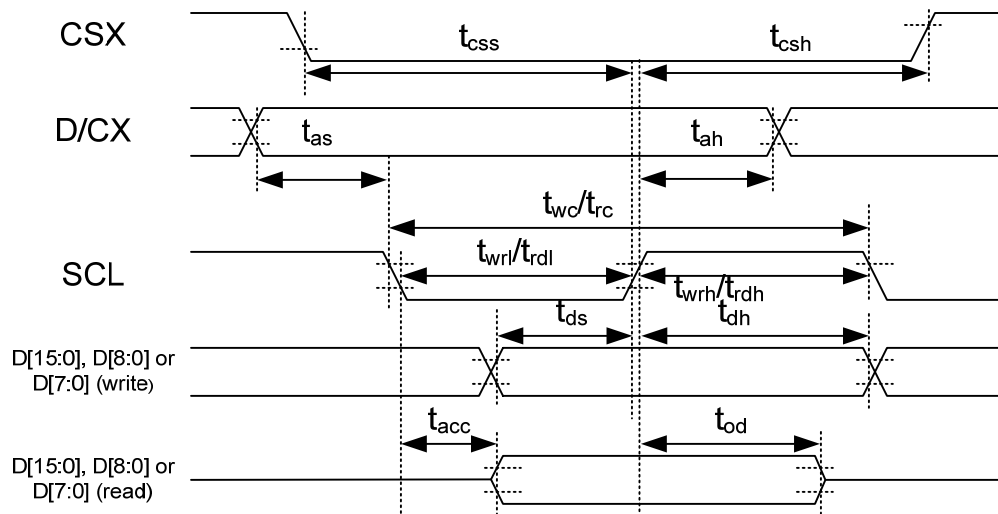
432

Table 9 AC Characteristics -- Type B Interface

Signal	Symbol	Parameter	min	max	Unit	Description
D/CX	t_{ast}	Address setup time	T	-	ns	
	t_{aht}	Address hold time (Write/Read)	T	-	ns	
CSX	t_{cs}	Chip Select setup time (Write)	2xT	-	ns	(2xT, 3xT, ..., 16xT)
	t_{rcs}	Chip Select setup time (Read)	2xT	-	ns	(2xT, 3xT, ..., 16xT)
	t_{csf}	Chip Select Wait time (Write/Read)	20	-	ns	
WRX	t_{wc}	Write cycle	5xT	79xT	ns	(5xT, 6xT, ..., 79xT)
	t_{wrh}	Write Control pulse H duration	3xT	63xT	ns	(3xT, 6xT, ..., 63xT)
	t_{wrl}	Write Control pulse L duration	2xT	16xT	ns	(2xT, 3xT, ..., 16xT)
RDX	t_{rc}	Read cycle	5xT	79xT	ns	(5xT, 6xT, ..., 79xT)
	t_{rdh}	Read Control pulse H duration	3xT	63xT	ns	(3xT, 6xT, ..., 63xT)
	t_{rdl}	Read Control pulse L duration	2xT	16xT	ns	(2xT, 3xT, ..., 16xT)
D[15:0], D[8:0], or D[7:0]	t_{wds}	Write data setup time	15	-	ns	For maximum $C_L=30\text{pF}$
	t_{wdh}	Write data hold time	25	-	ns	
	t_{racc}	Read access time	10	-	ns	For minimum $C_L=8\text{pF}$
	t_{rod}	Read output disable time	10	-	ns	

433 Note:

- 434 1. $T_a = -30$ to 70 °C, V_{DDI} range: according to Logic High level input voltage classification, GND =
435 0V, $T = 10 \pm 0.5$ ns
- 436 2. Does not include signal rise and fall times.



437

438

Figure 34 AC Characteristics, Type C Interface

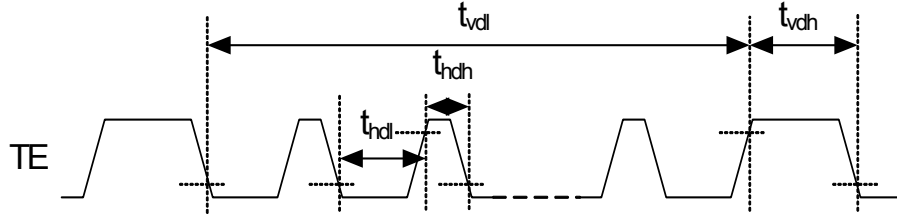
439

Table 10 AC Characteristics -- Type C Interface

Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip Select setup time (Write)	4xT	-	ns	
	tcsh	Chip Select setup time (Read)	4xT	-	ns	
D/CX (optional)	tas	Address setup time	T	-	ns	
	tah	Address hold time (Write/Read)	T	-	ns	
SCL(write)	twc	Write cycle	10xT	-	ns	
	twrh	SCL H duration (write)	4xT	-	ns	
	twrl	SCL L duration (write)	4xT	-	ns	
SCL(read)	trc	Read cycle	15xT	-	ns	
	trdh	SCL H duration (read)	6xT	-	ns	
	trdl	SCL L duration (read)	6xT	-	ns	
DOUT or SDA(write)	tds	Data setup time	3xT	-	ns	For maximum CL=30pF
	tdh	Data hold time	3xT	-	ns	
DIN or SDA(read)	tacc	Access time	10		ns	For minimum CL=8pF
	tod	Output disable time	T	5xT	ns	

440 Note:

- 441 1. $T_a = -30$ to 70 °C, V_{DDI} range: according to Logic High level input voltage classification, GND =
- 442 0V, $T = 10 \pm 0.5$ ns
- 443 2. Does not include signal rise and fall times



444

445

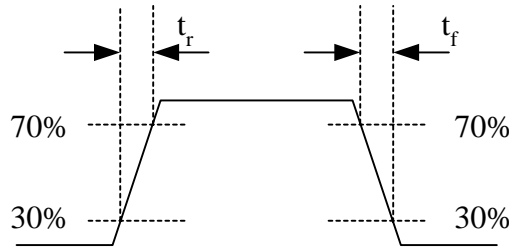
Figure 35 TE Timings

446

Table 11 Example TE Timing Values

Symbol	Parameter	min	max	Unit	Description
t_{vdl}	Vertical Timing Low Duration	DOI	-	ms	
t_{vdh}	Vertical Timing High Duration	1000	-	μ s	
t_{hdl}	Horizontal Timing Low Duration	DOI	-	μ s	
t_{hdh}	Horizontal Timing High Duration	24	500	μ s	

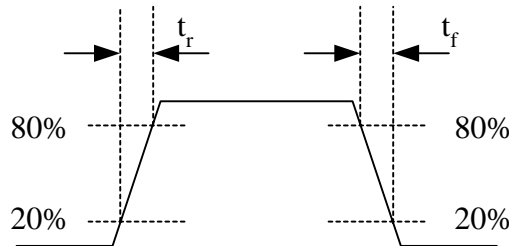
447 Note: $T_a = -30$ to 70 °C, V_{DDI} range: according to Logic High level input voltage classification, GND = 0V



448

449

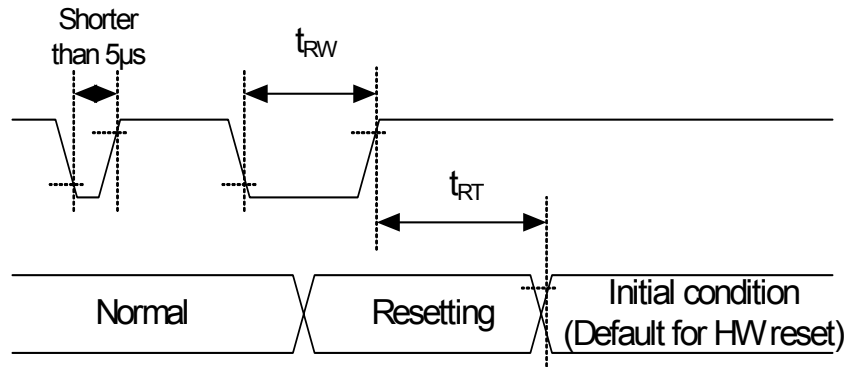
Figure 36 Signal Rise and Fall Times, Host to Display Module ($t_r \leq 15$ ns, $t_f \leq 15$ ns)



450

451

Figure 37 Signal Rise and Fall Times, Display Module to Host ($t_r \leq 15$ ns, $t_f \leq 15$ ns)



452

453

Figure 38 Example Reset Timings

454

Table 12 Example Reset Timing Values

Signal	Symbol	Parameter	Min	Max	Unit
RESX	t_{RW}	Reset pulse duration	10		μs
	t_{RT}	Reset cancel		5	ms

455 Notes:

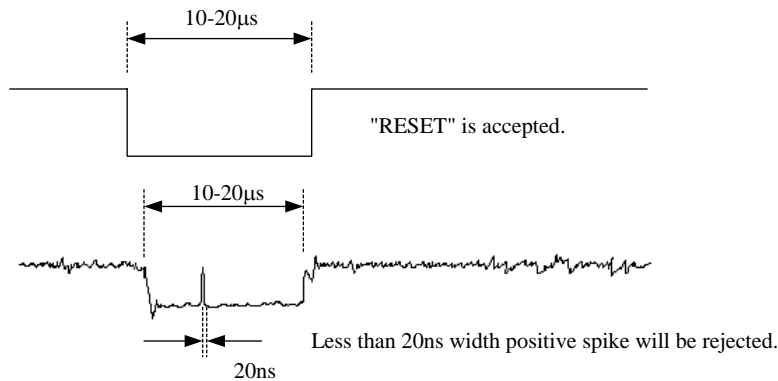
456 1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset
 457 according to Table 13.

458 2. Spike Rejection also applies during a valid reset pulse as shown below:

459

Table 13 RESX Pulse Conditions

RESX Pulse	Action
Shorter than $5\mu s$	Reset Rejected
Longer than $9\mu s$	Reset
Between $5\mu s$ and $9\mu s$	Reset starts



460

461

Figure 39 RESX Input Spike Rejection

462 **9 Reset**463 **9.1 Host Input/Output Pins**464 **9.1.1 Input Pins, I/O Pins**465 **Table 14 Host Input and I/O Pin Status Corresponding to Reset and Power On/Off Process**

Signal Line	During Display Power-on Process	After Powered On	After Hardware Reset	During Display Module Power Off Process
TE Line	Input Invalid	Input Valid	Input Valid	Input Invalid
D[15:0], D[8:0], D[7:0], SDA (input) or DIN	Input Invalid	Input Valid	Input Valid	Input Invalid

466 **9.1.2 Output Pins**467 **Table 15 Host Output Pin Status Corresponding to Reset and Power On/Off Process**

Signal Line	During Display Power-on Process	After Powered On	After Hardware Reset	During Display Module Power Off Process
RESX	Low	High	High	Low
CSX	High	High	High	High
D/CX	High or Low	High or Low	High or Low	High or Low
R/WX	High or Low	High or Low	High or Low	High or Low
E	High or Low	High or Low	High or Low	High or Low
WRX	High or Low	High	High	High
RDX	High	High	High	High
SCL	High or Low	High	High	High
D[15:0], D[8:0], D[7:0], SDA (output) or DOUT	High-Z (Inactive) or Low	High-Z (Inactive) or Low	High-Z (Inactive) or Low	High-Z (Inactive) or Low

468

469 **9.2 Display Input/Output Pins**470 **9.2.1 Output Pins, I/O Pins**471 **Table 16 Display Output and I/O pin Status After Reset and Power On/Off Process**

Signal Line	After Powered On	After Hardware Reset
TE Line	Low	Low
D[15:0], D[8:0], D[7:0], SDA (output) or DIN	High-Z (Inactive)	High-Z (Inactive)

472 Note: There will be no output from D[15:0] or D[7:0] during Power On/Off sequences and Hardware Reset.

473 **9.2.2 Input Pins**474 **Table 17 Display Input Pin Status Corresponding to Reset and Power On/Off Process**

Signal Line	During Display Power On Process	After Powered On	After Hardware Reset	During Display Power Off Process
RESX	DOI	Input valid	Input valid	DOI
CSX	Input invalid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input invalid
R/WX	Input invalid	Input valid	Input valid	Input invalid
E	Input invalid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input invalid
SCL	Input invalid	Input valid	Input valid	Input invalid
D[15:0], D[8:0], D[7:0], SDA (input) or DOUT	Input invalid	Input valid	Input valid	Input invalid

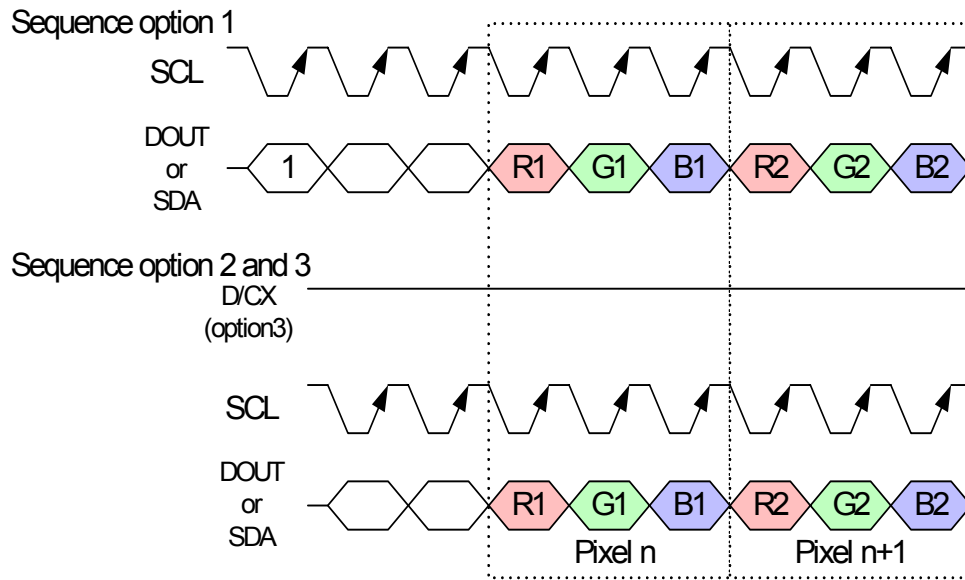
475

476 **10 Interface Color Coding**

477 Color coding uses a red [R], green [G] and blue [B] additive color mixing method. R, G and B are used for
 478 each color data index in the following sections.

479 **10.1 Serial Interface**

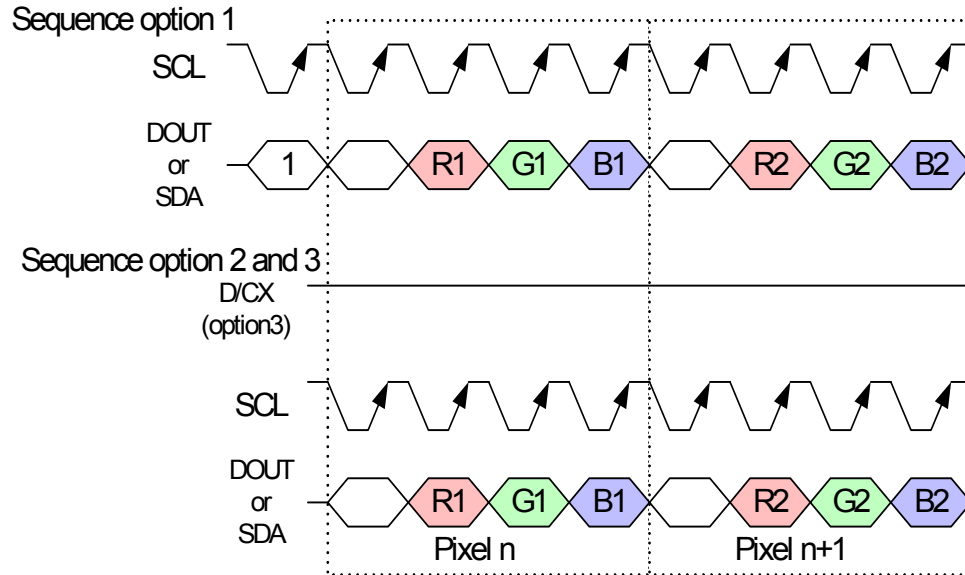
480 **10.1.1 3-bits/pixel (R 1-bit, G 1-bit, B 1-bit), Eight Colors - Option1**



481
 482

Figure 40 3-bits/pixel (R 1-bit, G 1-bit, B 1-bit), Eight Colors - Option 1

483 **10.1.2 3-bit/pixel (R 1-bit, G 1-bit, B 1-bit), Eight Colors – Option 2**



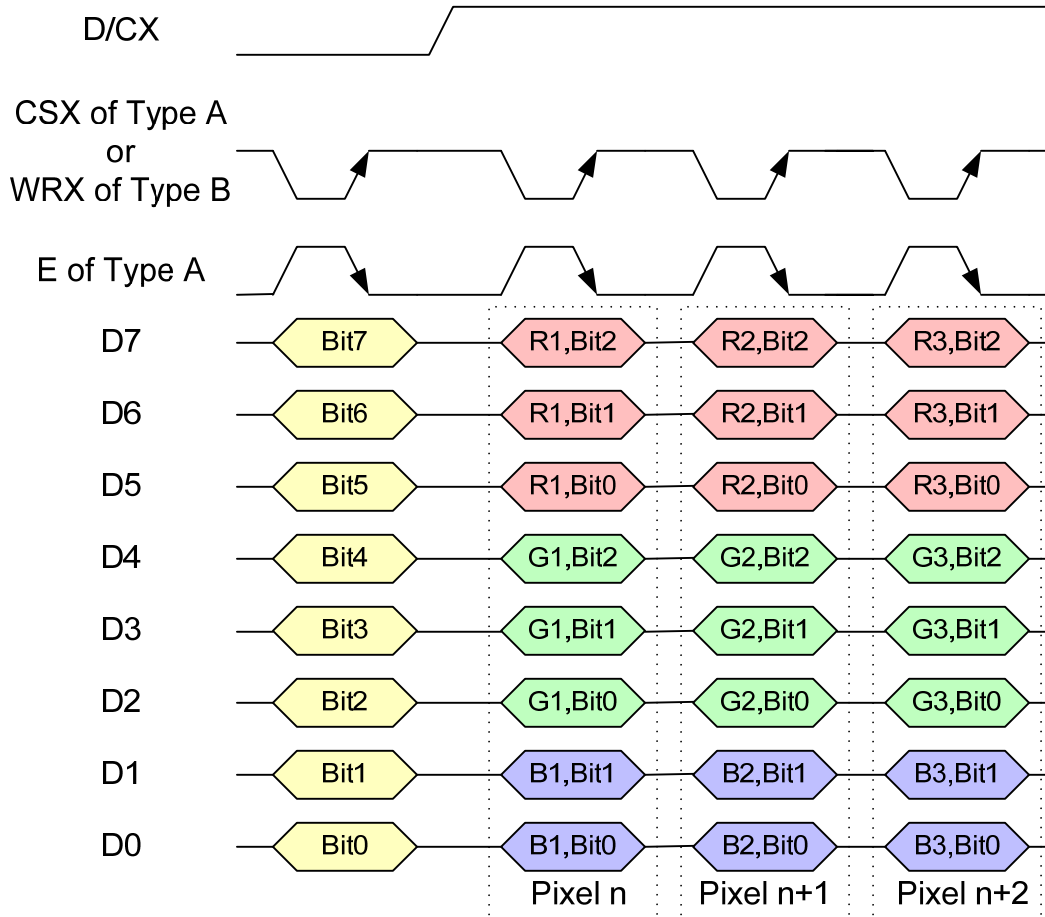
484

485

Figure 41 3-bit/pixel (R 1-bit, G 1-bit, B 1-bit), Eight Colors - Option 2

486 **10.2 8-bit Interface**

487 **10.2.1 8-bits/pixel (R 3-bit, G 3-bit, B 2-bit), 256 Colors**



488

489

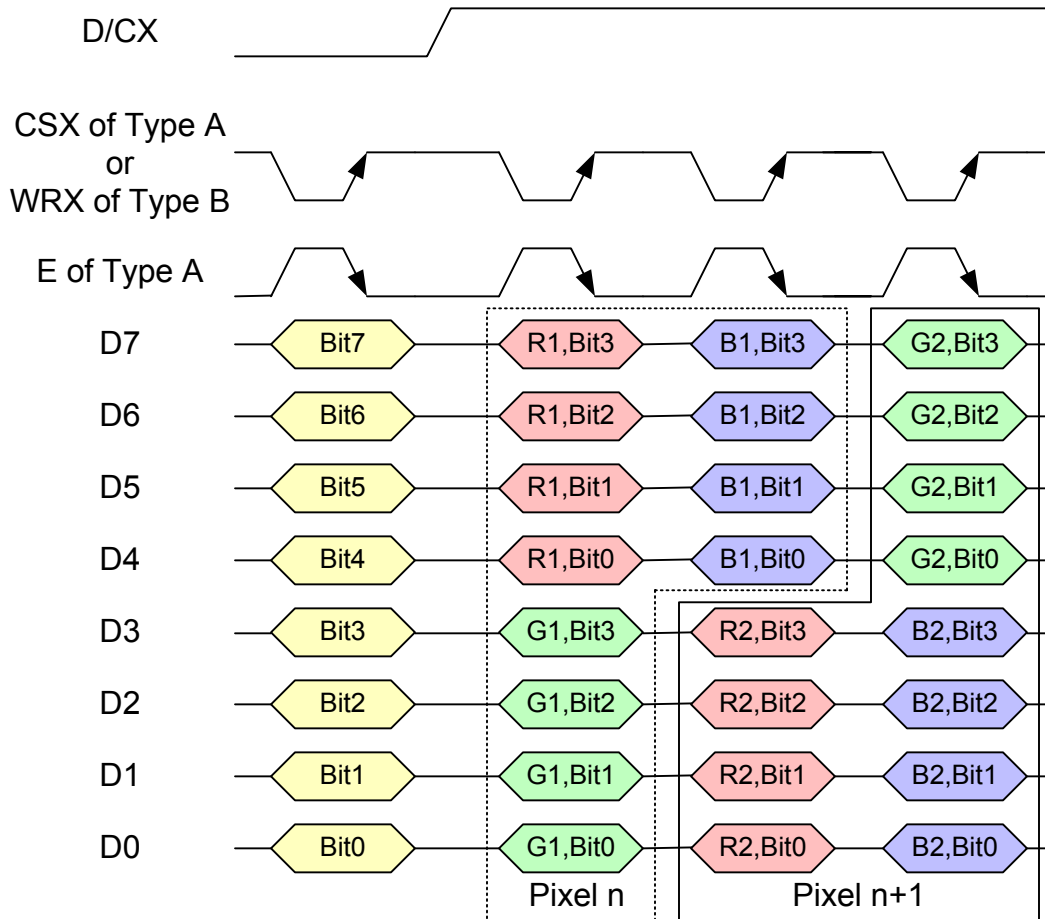
Figure 42 8-bits/pixel (R 3-bit, G 3-bit, B 2-bit), 256 Colors

490

Note: The Data order is as follows, MSB = D7, LSB = D0. Picture Data is MSB = Bit2, LSB = Bit0 for Red and Green data, MSB = Bit1, LSB = Bit0 for Blue data.

491

492 **10.2.2 12-bits/pixel (R 4-bit, G 4-bit, B 4-bit), 4,096 Colors**



493

494

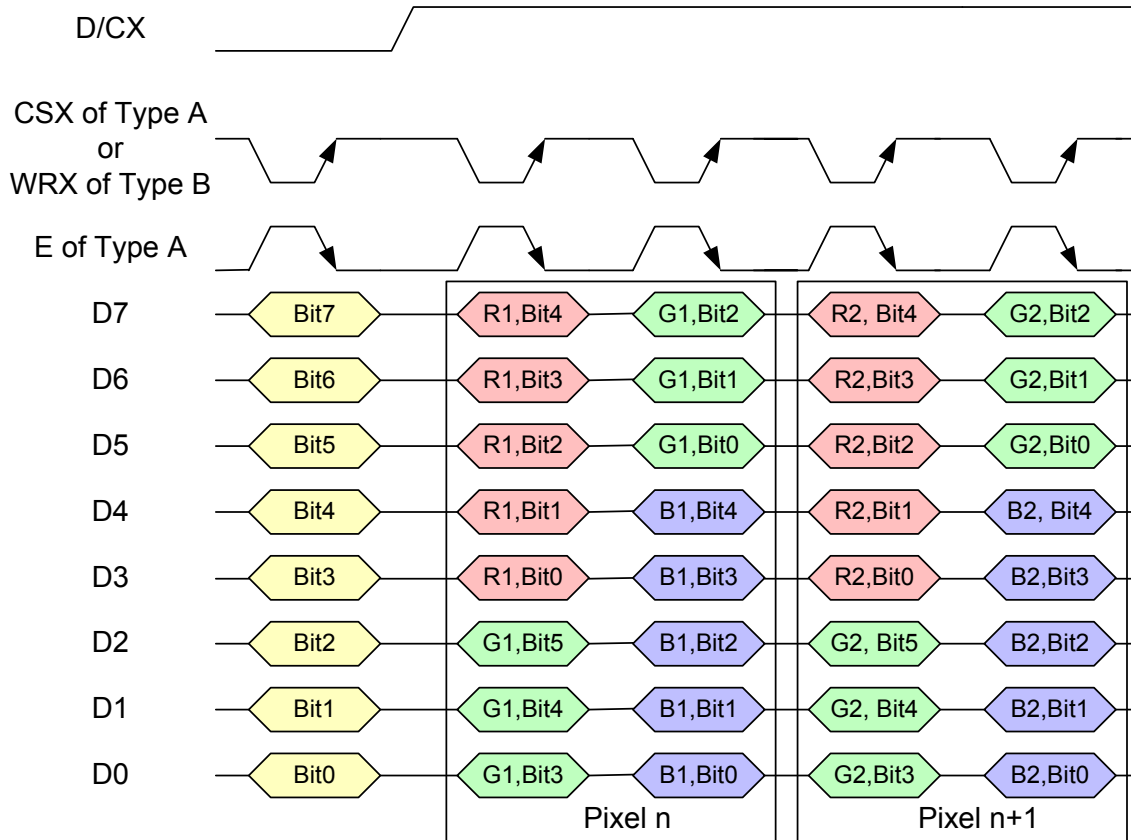
Figure 43 12-bits/pixel (R 4-bit, G 4-bit, B 4-bit), 4,096 Colors

495

Note: The Data order is as follows, MSB = D7, LSB = D0. Picture Data is MSB = Bit3, LSB = Bit0 for Red, Green, and Blue data.

496

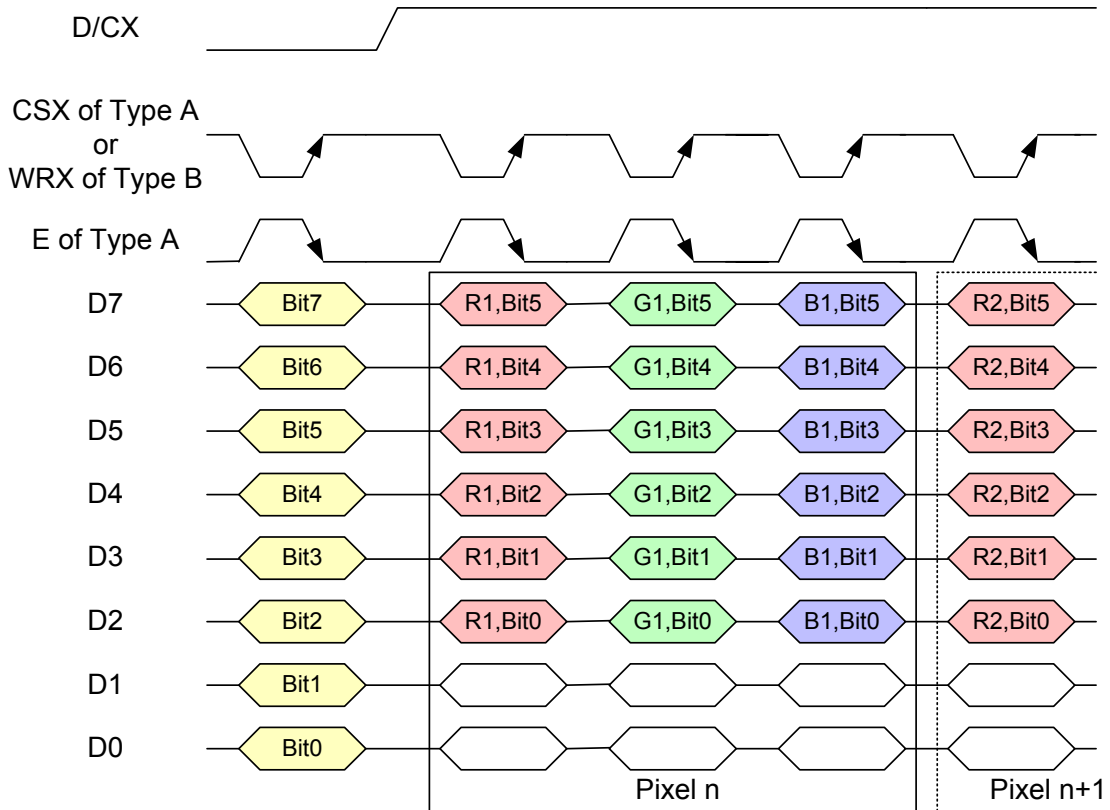
497 **10.2.3 16-bits/pixel (R 5-bit, G 6-bit, B 5-bit), 65,536 Colors**



498 **Figure 44 16-bits/pixel (R 5-bit, G 6-bit, B 5-bit), 65,536 Colors**

500 Note: The Data order is as follows, MSB = D7, LSB = D0. Picture Data is MSB = Bit5, LSB = Bit0 for
 501 Green data, MSB = Bit4, LSB = Bit0 for Red and Blue data.

502 **10.2.4 18-bits/pixel (R 6-bit, G 6-bit, B 6-bit), 262,144 Colors**



503

504

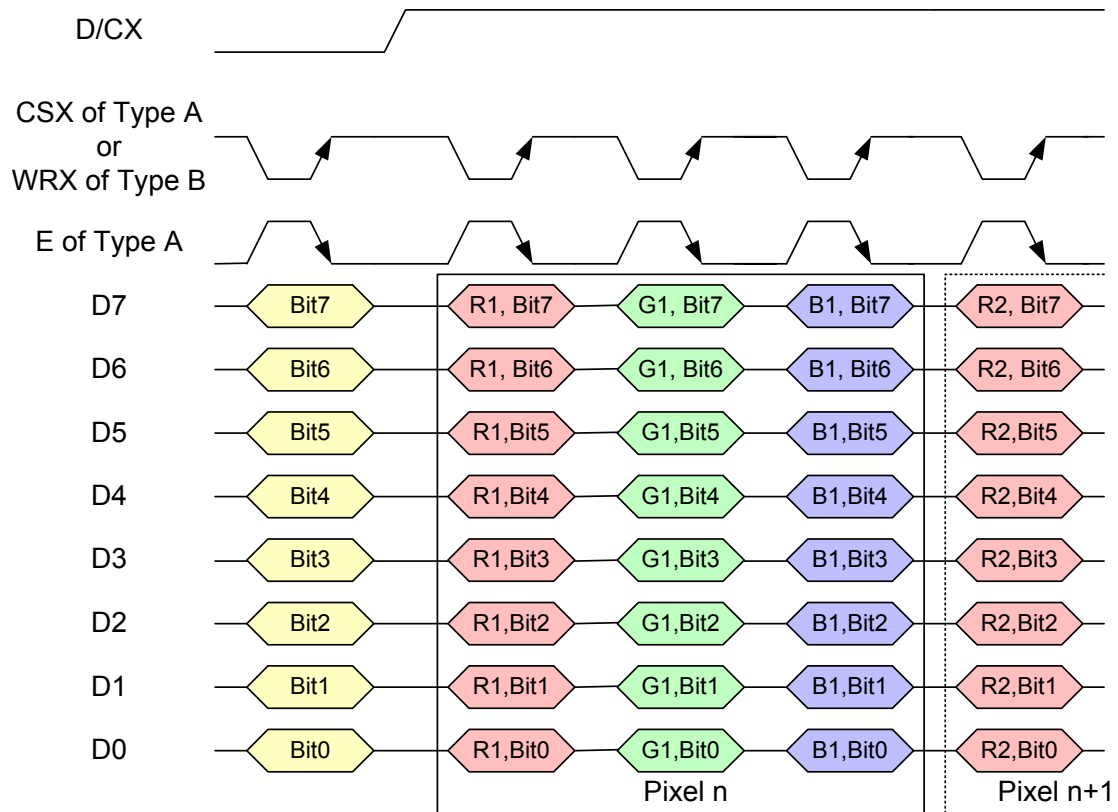
Figure 45 18-bits/pixel (R 6-bit, G 6-bit, B 6-bit), 262,144 Colors

505

Note: The Data order is as follows, MSB = D7, LSB = D0. Picture Data is MSB = Bit5, LSB = Bit0 for Red, Green, and Blue data.

506

507 **10.2.5 24-bits/pixel (R 8-bit, G 8-bit, B 8-bit), 16,777,216 Colors**



508

509

Figure 46 24-bits/pixel (R 8-bit, G 8-bit, B 8-bit), 16,777,216 Colors

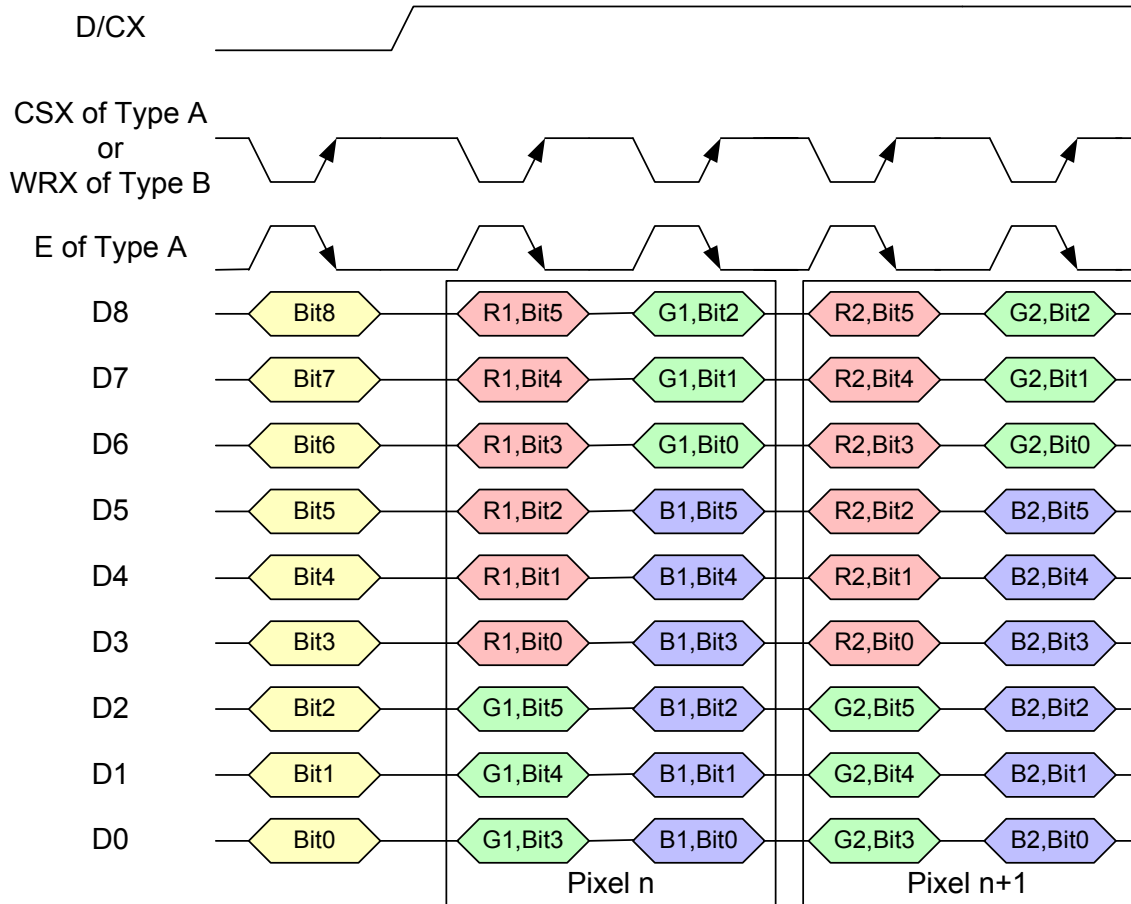
510

Note: The Data order is as follows, MSB = D7, LSB = D0. Picture Data is MSB = Bit7, LSB = Bit0 for Red, Green, and Blue data.

511

512 **10.3 9-bit interface**

513 **10.3.1 18-bits/pixel (R 6-bit, G 6-bit, B 6-bit), 262,144 Colors**



514

515

Figure 47 18-bits/pixel (R 6-bit, G 6-bit, B 6-bit), 262,144 Colors

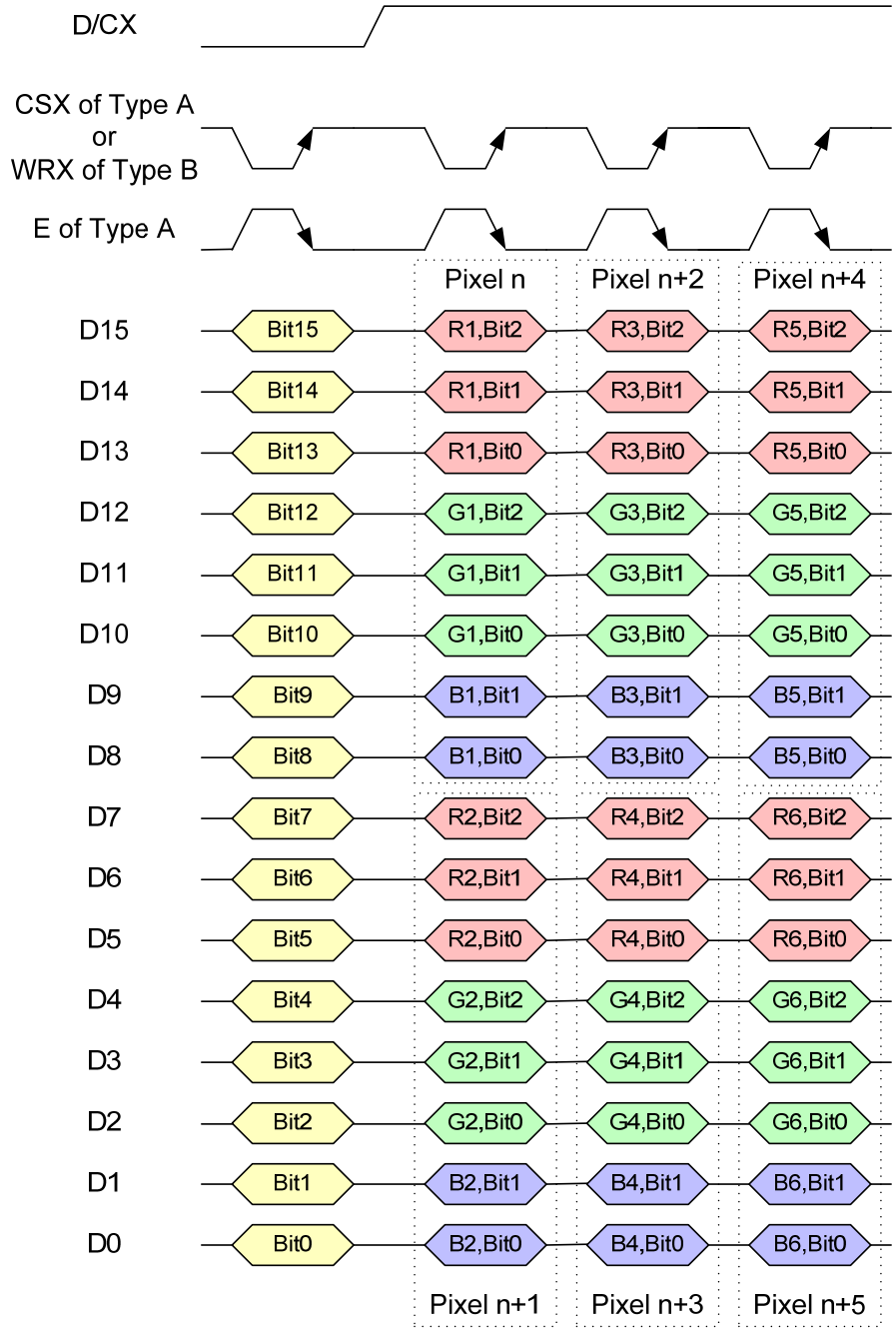
516

Note: The Data order is as follows, MSB = D8, LSB = D0. Picture Data is MSB = Bit5, LSB = Bit0 for Red, Green, and Blue data.

517

518 **10.4 16-bit Interface**

519 **10.4.1 8-bits/pixel (R 3-bit, G 3-bit, B 2-bit), 256 Colors**



520

521

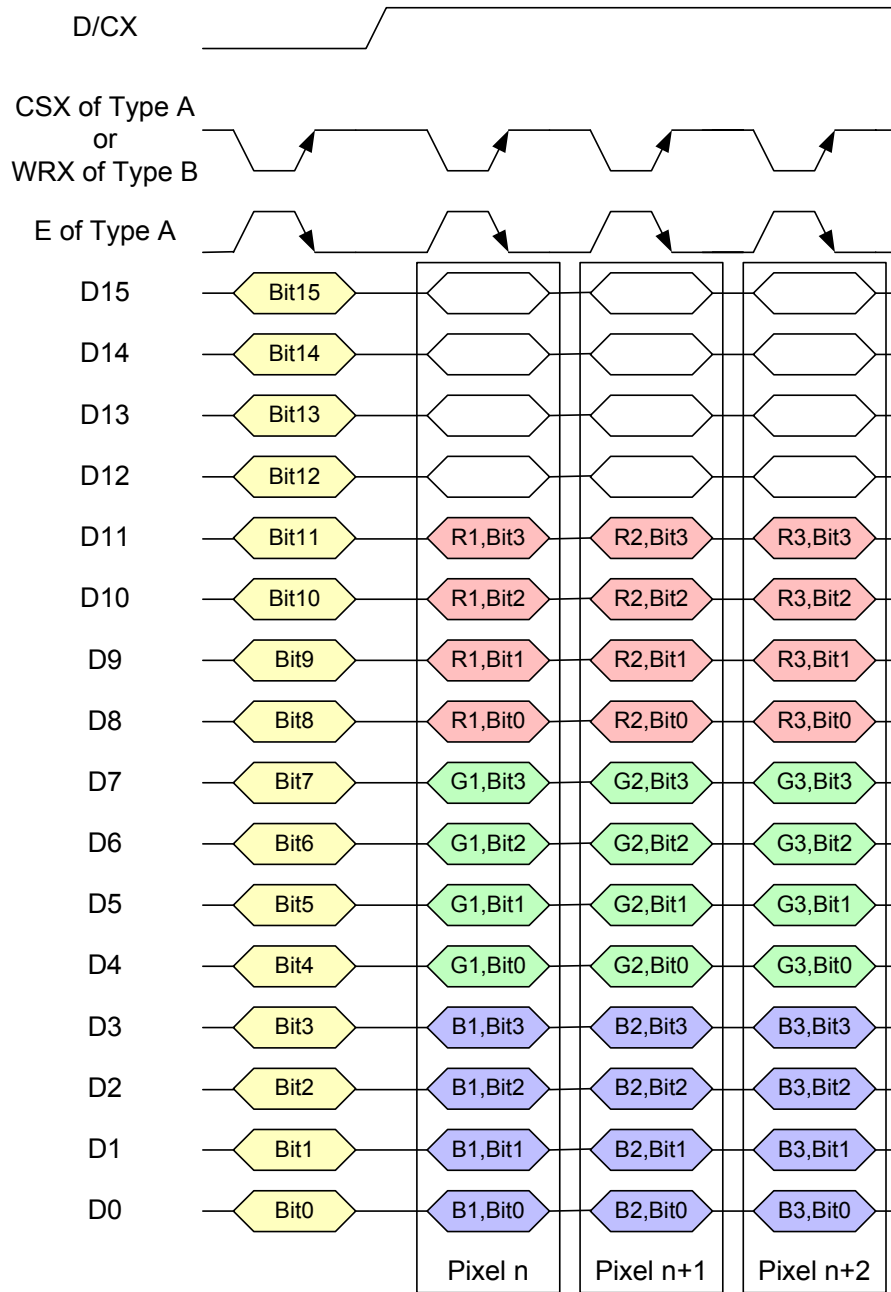
Figure 48 8-bits/pixel (R 3-bit, G 3-bit, B 2-bit), 256 Colors

522

Note: The Data order is as follows: MSB = D15, LSB = D0 and image data is MSB = Bit2, LSB = Bit0 for Red and Green data, and MSB = Bit1, LSB = Bit0 for Blue data.

523

524 **10.4.2 12-bits/pixel (R 4-bit, G 4-bit, B 4-bit), 4,096 Colors**



525

526

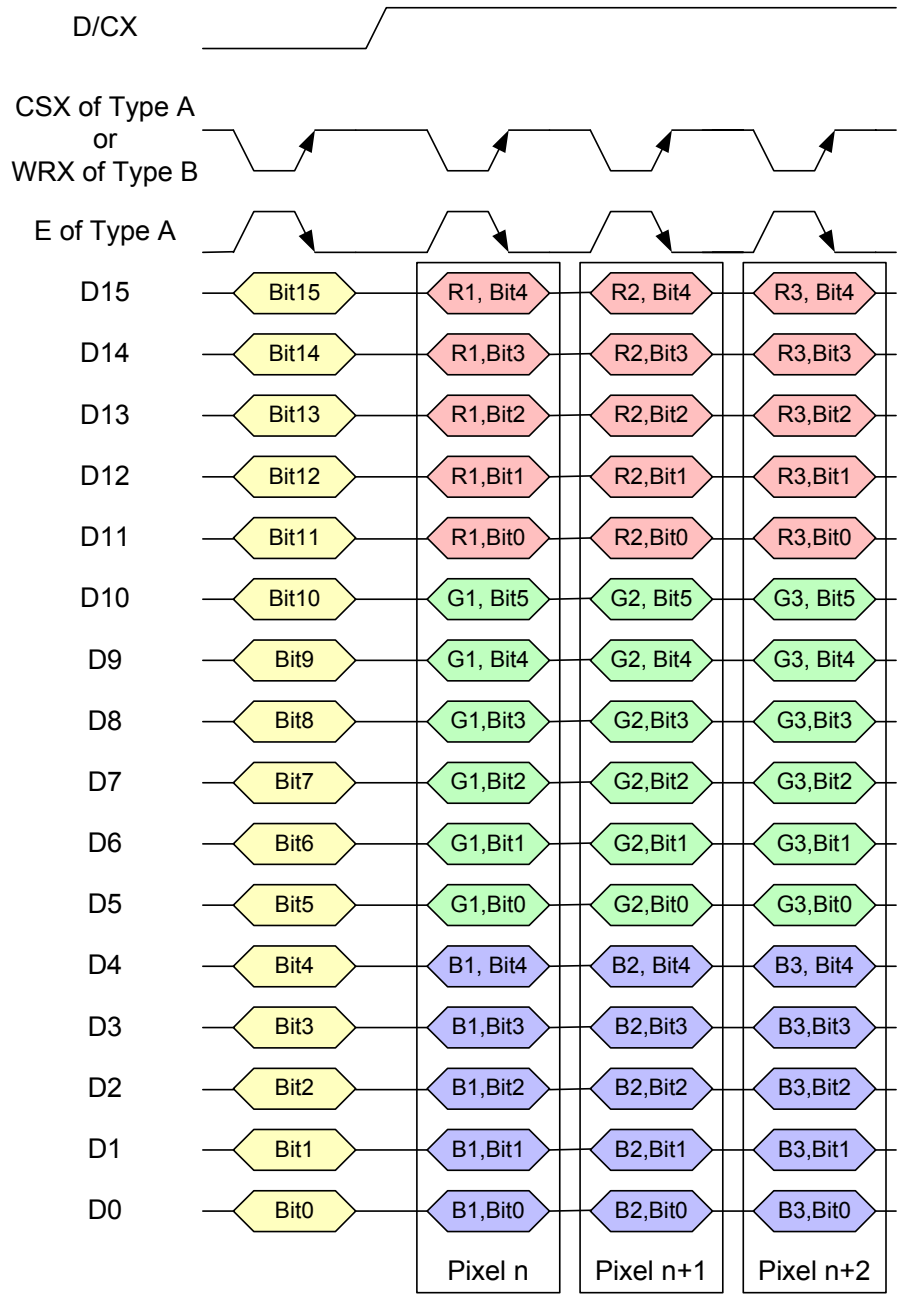
Figure 49 12-bits/pixel (R 4-bit, G 4-bit, B 4-bit), 4,096 Colors

527

Note: The Data order is as follows, MSB = D15, LSB = D0 and image data is MSB = Bit3, LSB = Bit0 for Red, Green, and Blue data.

528

529 **10.4.3 16-bits/pixel (R 5-bit, G 6-bit, B 5-bit), 65,536 Colors**



530

531

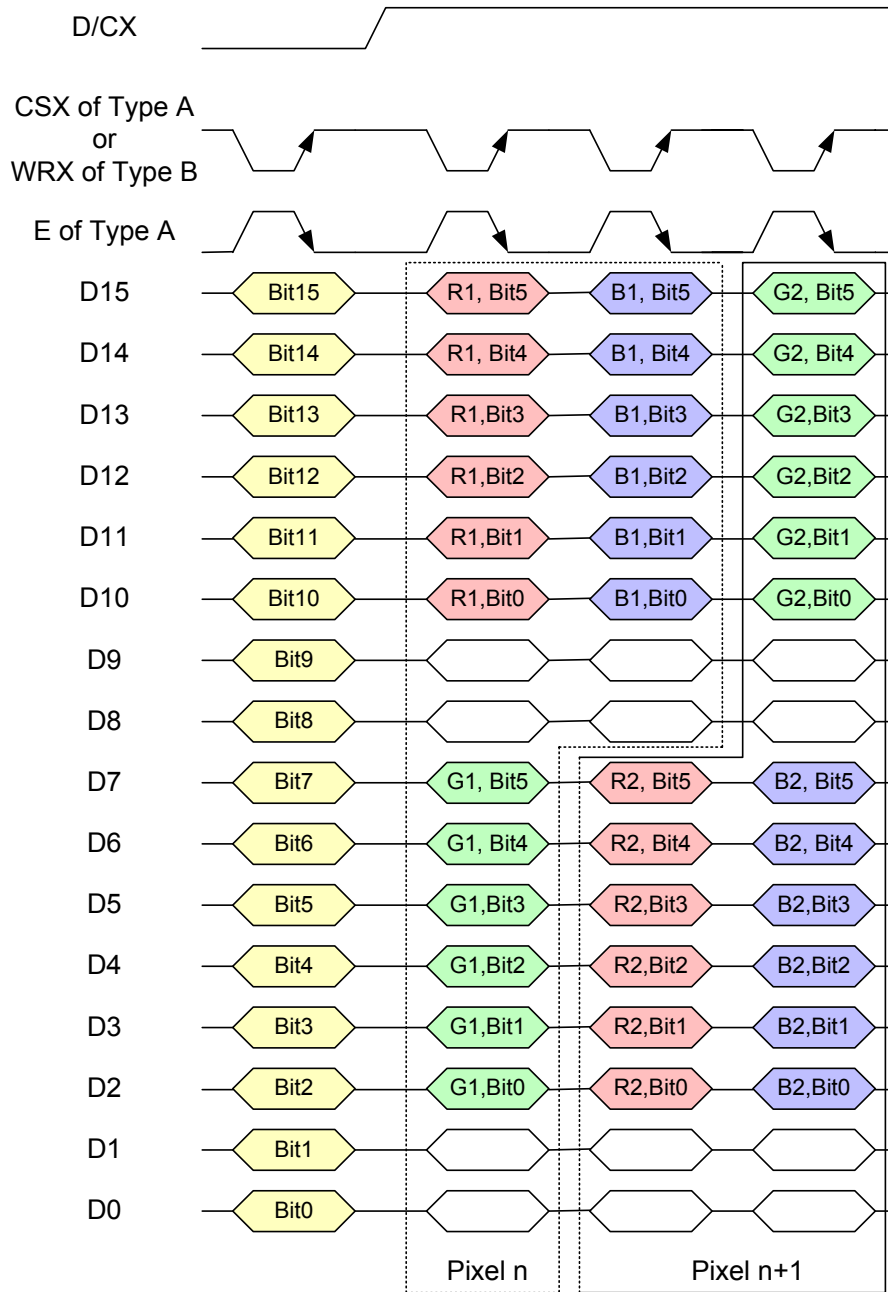
Figure 50 16-bits/pixel (R 5-bit, G 6-bit, B 5-bit), 65,536 Colors

532

Note: The Data order is as follows, MSB = D15, LSB = D0 and image data is MSB = Bit5, LSB = Bit0 for Green data and MSB = Bit4, LSB = Bit0 for Red and Blue data.

533

534 **10.4.4 18-bits/pixel (R 6-bit, G 6-bit, B 6-bit), 262,144 Colors - Option 1**



535

536

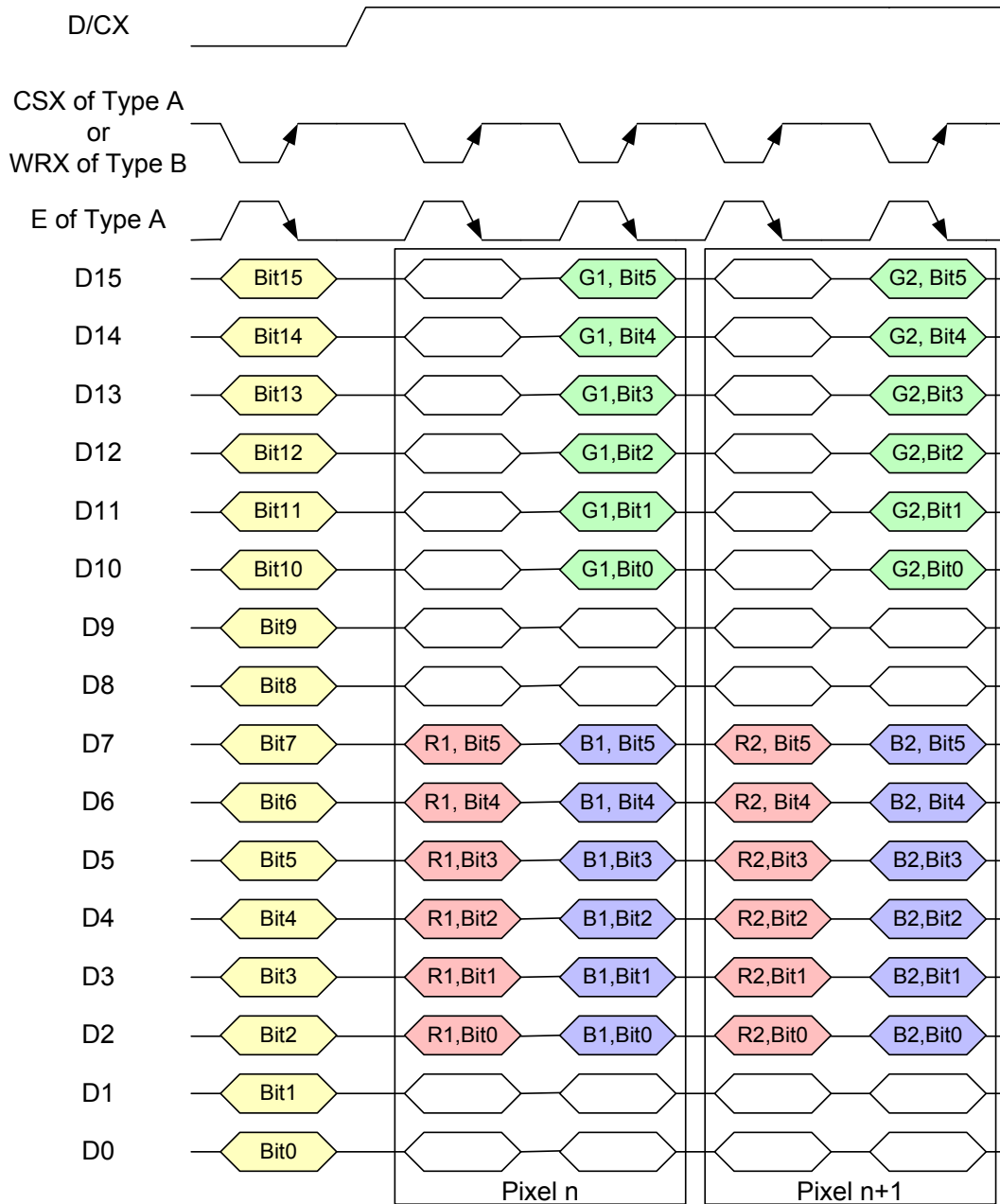
Figure 51 18-bits/pixel (R 6-bit, G 6-bit, B 6-bit), 262,144 Colors

537

Note: The Data order is as follows, MSB = D15, LSB = D0 and image data is MSB = Bit5, LSB = Bit0 for Red, Green, and Blue data.

538

539 10.4.5 18-bits/pixel (R 6-bit, G 6-bit, B 6-bit), 262,144 Colors - Option 2



540

541

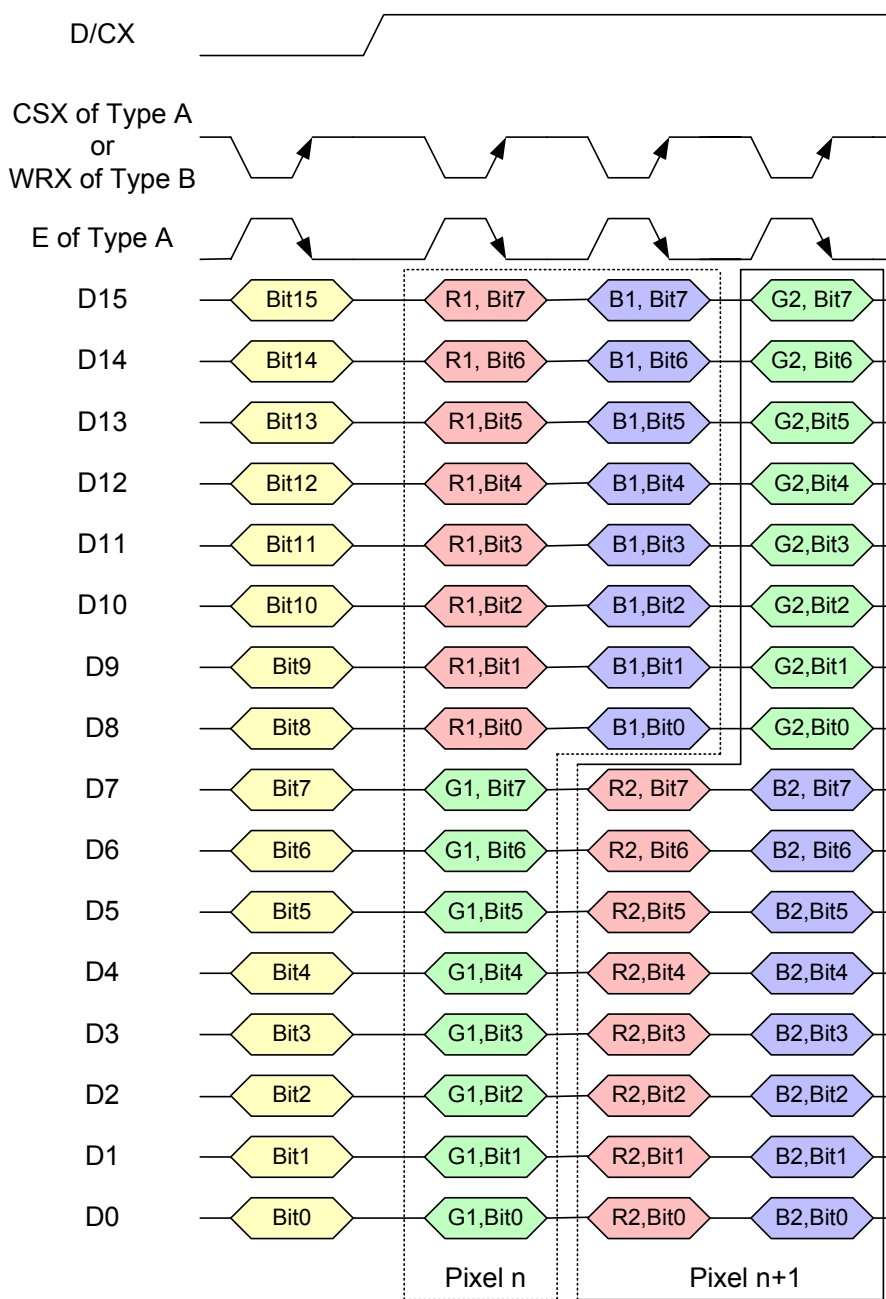
Figure 52 18-bits/pixel (R 6-bit, G 6-bit, B 6-bit), 262,144 Colors

542

Note: The Data order is as follows, MSB = D15, LSB = D0 and image data is MSB = Bit5, LSB = Bit0 for Red, Green, and Blue data.

543

544 **10.4.6 24-bits/pixel (R 8-bit, G 8-bit, B 8-bit), 16,777,216 Colors - Option 1**



545

546

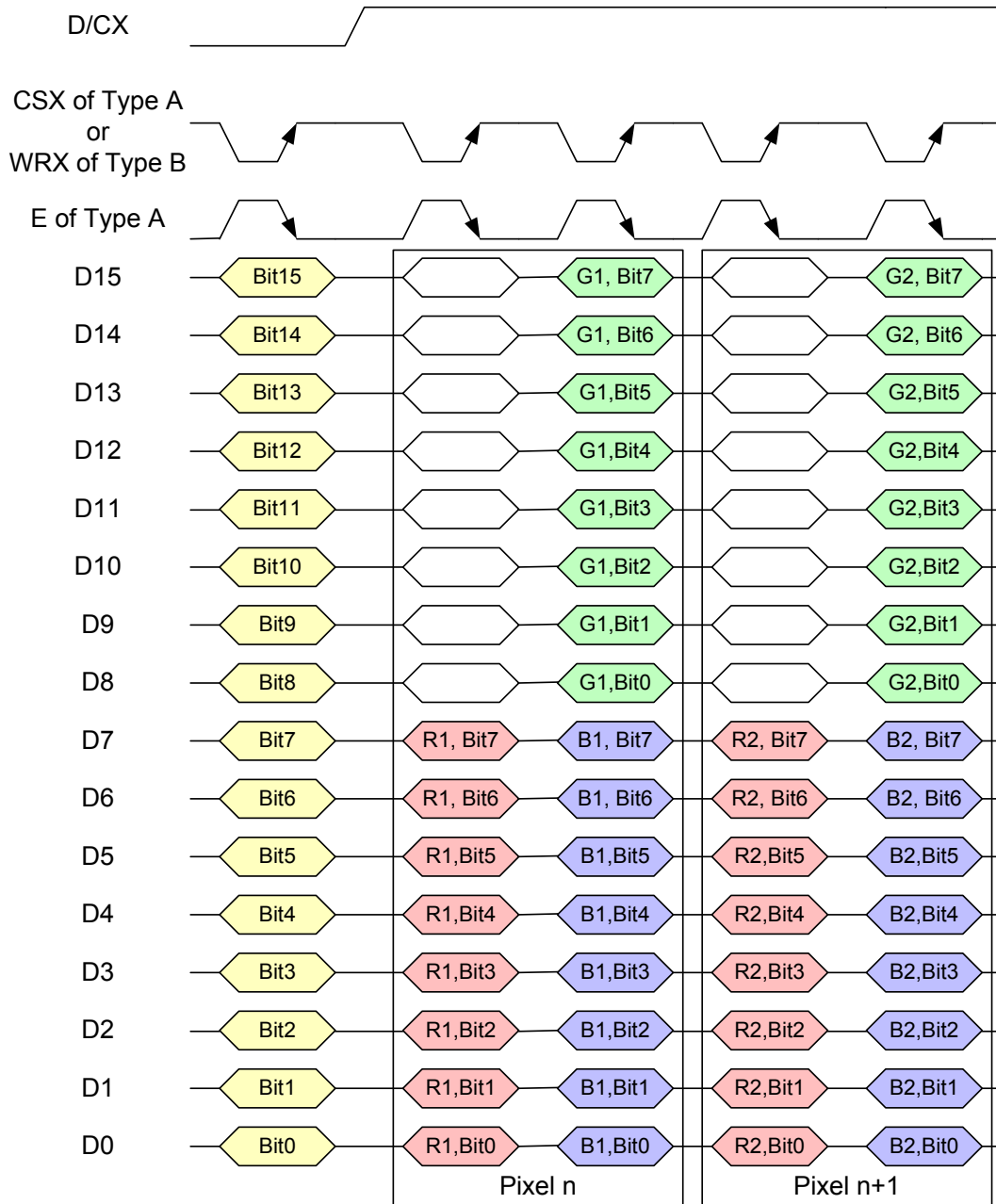
Figure 53 24-bits/pixel (R 8-bit, G 8-bit, B 8-bit), 16,777,216 Colors

547

Note: The Data order is as follows, MSB = D15, LSB = D0 and image data is MSB = Bit7, LSB = Bit0 for Red, Green, and Blue data.

548

549 10.4.7 24-bits/pixel (R 8-bit, G 8-bit, B 8-bit), 16,777,216 Colors - Option 2



550

Figure 54 24-bits/pixel (R 8-bit, G 8-bit, B 8-bit), 16,777,216 Colors

551

552 Note: The Data order is as follows, MSB = D15, LSB = D0 and image data is MSB = Bit7, LSB = Bit0 for
553 red, Green, and Blue data.

554 **11 Command Set**

555 See the *MIPI Alliance Standard for Display Command Set* for a description of the commands in order to
556 control the display module through DBI.

557 **12 Interoperability, and Optional Capabilities**

558 This section describes interoperability requirements between different host processors and displays in DBI
559 application. There are a number of categories of potential differences or attributes that must be considered
560 to ensure interoperability between a host processor and a display module in DBI usage.

561 1. DBI implementation Types A, B and C

562 Each host processor and display module shall implement one or more of Type A, B or C interfaces.

563 2. TE support in Type A implementations

564 Each host processor or display module may support TE when the Type A interface is implemented.

565 3. Type C option 1, 2 and 3 as specified in section 4.

566 Each host processor and display module shall implement one or more options of Option 1, 2 and 3
567 when it implements a type C interface.

568 4. Logic High level input voltage classification

569 Each host processor and display module shall support one or more voltage classification of Class 1, 2,
570 3 or 4.

571 5. Interface color coding

572 Each host processor shall support one or more color coding scheme of 8-, 12-, 16-, 18- or 24-bits per
573 pixel when a Type 1 architecture is implemented.

574 Each display module shall support one or more color coding scheme of 8-, 12-, 16-, 18- or 24-bits per
575 pixel, up to its native number of colors, when a Type 1 architecture is implemented.

576 Each host processor and display module shall support 3-bits per pixel when a Type 2 or 3 architecture
577 is implemented.

578 6. Bus width option Type A and Type B

579 Each host processor and display module shall support one or more bus width options of 8-, 9- and 16-
580 bits.