MIPI Alliance Standard for Display Pixel Interface (DPI-2)

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Contents

MIPI Alliance Standard for Display Pixel Interface

1 Overview

This document describes Display Pixel Interface (DPI), which is used for Active-Matrix LCD displays for handheld devices. The interface may be configured with data path of 16, 18 or 24 parallel data bits, and several control signals.

This document specifies the interface requirements for both ends (host and display) of the link, including the following attributes:

- Electrical
- Timing
- Pixel formats (mapping of pixel bits to data signals)
- Command set to control display behaviors

1.1 Scope

The scope of this document is to specify an electrical and logical interface between a host system (processor or controller) and an active-matrix (AM) display module. The specification is intended for display modules in mobile devices, with display resolution up to 800x480 pixels. This specification does not apply to passive-matrix display modules.

Included, and within the scope of this specification, is the power supply for interface signaling between the host processor and the display module. However, power supply for other functions in the display module are beyond the scope of this specification.

1.2 Purpose

The Display Pixel Interface specification is used by manufacturers to design products that adhere to MIPI specifications for mobile device processor, camera and display interfaces.

Implementing the DPI standard reduces the time-to-market and design cost of mobile devices by simplifying the interconnection of products from different manufacturers. In addition, adding new features such as larger or additional displays to mobile devices is simplified due to the extensible nature of the MIPI specifications.

2 Terminology

2.1 Definitions

Command: Digital information used to control display behavior and to identify the connected display module

Data: Digital image data stored in the frame memory or numerical information to define the display module behavior accompanied with a command

Display Controller: Isolated IC silicon chip or integrated functional block in the host processor to control a display module; may or may not include frame memory

Display Device: Functional device which can show image, such as Liquid Crystal Displays

Display Driver IC: IC silicon chip in a display module used to control the display device; may or may not include frame memory

Display Glass: Same as display device, coming from material name

Display Module: Functional module to show image on it, can consists of display device, display driver IC, other peripheral components and circuits and display interface

Display Panel: Same as Display Device, coming from the physical outward appearance of the display device

Frame Memory: Memory device integrated in a display driver IC or display controller in order to provide image data for refreshing the display device. Full-frame memory provides a full screen area of image data while partial-frame memory only provides memory for a portion of the screen area.

Type 1 Display Architecture: One of the defined display module architectures. In DSI, DBI, DPI, and DCS, a display module architecture in which a display module includes a display device, display driver IC, full-frame memory, registers, timing controller, non-volatile memory and control interface.

Type 2 Display Architecture: One of the defined display module architectures. In DSI, DBI, DPI, and DCS, a display module architecture in which a display module includes a display device, display driver IC, partial-frame memory, registers, timing controller, non-volatile memory, control interface and video stream interface.

Type 3 Display Architecture: One of the defined display module architectures. In DSI, DBI, DPI, and DCS, a display module architecture in which a display module includes a display device, display driver IC, registers, timing controller, non-volatile memory, control interface and video stream interface.

Type 4 Display Architecture: One of the defined display module architectures. In DSI, DBI, DPI, and DCS, a display module architecture in which a display module includes a display device, display driver IC, registers, timing controller, control lines and video stream interface.

2.2 Abbreviations

High-Z High Impedance

H-Sync Horizontal Synchronization

123	Ta	Ambient Temperature
124	VDD	Power Supply
125	V_{DDI}	Logic Level Supply
126	V-Sync	Vertical Synchronization

127 2.3 Acronyms

128	AGND	Analog ground, for power connection
129	AM	Active Matrix
130	ASIC	Application Specific Integrated Circuit
131	CM	Color Mode
132	CMOS	Complementary Metal Oxide Semiconductor
133	DBI	Display Bus Interface
134	DCS	Display Command Set
135	DE	Data Enable
136	DGND	Logic ground, for power connection
137	DOI	Dependent On Implementation
138	HBP	Horizontal Back Porch
139	HFP	Horizontal Front Porch
140	I/O	Input/Output
141	LCD	Liquid Crystal Display
142	LSB	Least Significant Bit
143	MIPI	Mobile Industry Processor Interface
144	MSB	Most Significant Bit
145	PCLK	Pixel Clock
146	SD	Shutdown
147	VBP	Vertical Back Porch
148	VFP	Vertical Front Porch

3 References

[1] MIPI Alliance Standard for Display Command Set, version 0.36, June 2005

[2] MIPI Alliance Standard for Display Bus Interface, version 0.xx, August 2005

4 Display Architectures and Interface Constructions

4.1 Display Architectures

The display module shall be based on Type 1, Type 2, Type 3 or Type 4 display architecture.

The Type 1 Display Architecture should consist of the following functional blocks:

Display Device. Used to show the image data.

Display Driver. May be one or more devices used to drive the display device.

Full-frame memory. Used to hold the image data; can be integrated in the display driver.

Registers. Used to configure the display module behavior and hold identification information; can be integrated in the display driver.

Timing Controller. Provides timing signals to control the display device and display driver based on configuration information; can be integrated in the display driver.

Non-volatile memory. Used to store default register and configuration values; can be integrated in the display driver.

Control Interface. Provides the interface between the host processor and the display driver; can be integrated in the display driver.

Display Driving Circuit. As a part of display driver, used to convert timing signals and voltages to signals appropriate to drive the display device.

Power Supply. Used to convert system voltages to levels usable by the display device and display driver; can be integrated in the display driver.

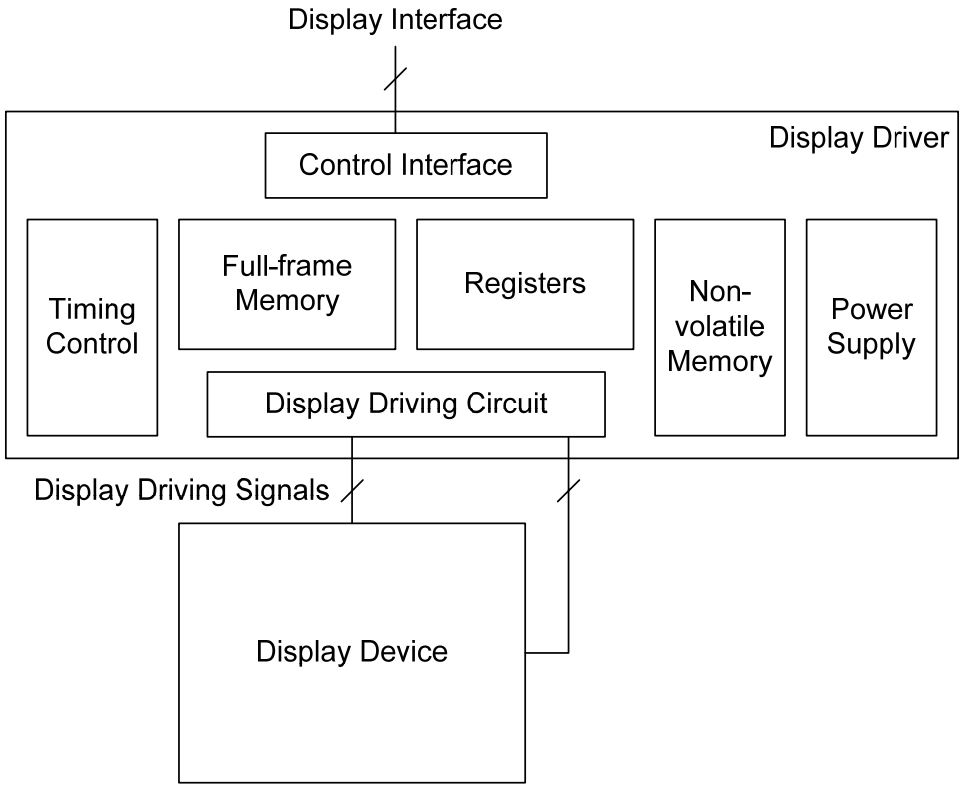


Figure 1 Type 1 Display Architecture Block Diagram

The Type 2 Display Architecture should consist of the following functional blocks:

Display Device. Used to show image data.

Display Driver. May be one or more devices used to drive the display device.

Partial-frame memory. Used to hold image data. Can be integrated in the display driver.

Registers. Used to configure the display module behavior and hold identification information; can be integrated in the display driver.

Timing Controller. Provides timing signals to control the display device and display driver based on configuration information; can be integrated in the display driver.

Non-volatile memory. Used to store default register and configuration values; can be integrated in the display driver.

Control Interface. Provides the interface between the host processor and the display driver; can be integrated in the display driver.

Display Driving Circuit. As a part of display driver, used to convert timing signals and voltages to signals appropriate to drive the display device.

Power Supply. Used to convert system voltages to levels usable by the display device and display driver; can be integrated in the display driver.

Video Stream Interface. Used to receive video image data and timing signals from the host processor.

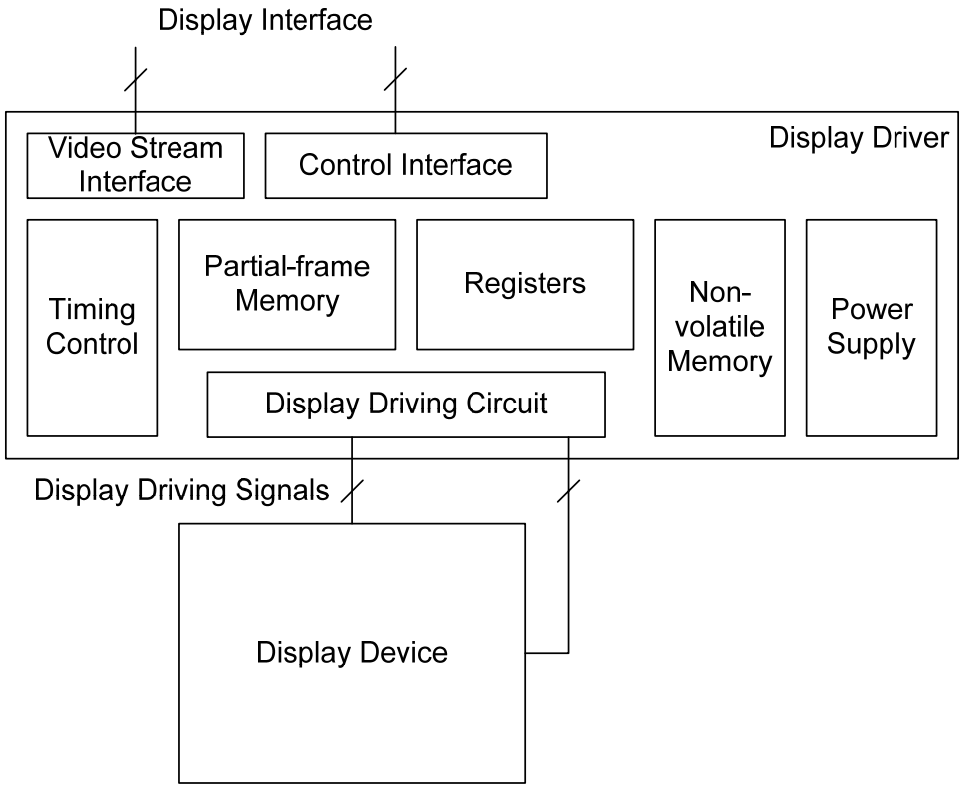


Figure 2 Type 2 Display Architecture Block Diagram

The Type 3 Display Architecture should consist of the following functional blocks:

Display Device. Used to show image data.

Display Driver. May be one or more devices used to drive the display device.

Registers. Used to configure the display module behavior and hold identification information; can be integrated in the display driver.

Timing Controller. Provides timing signals to control the display device and display driver based on configuration information; can be integrated in the display driver.

Non-volatile memory. Used to store default register and configuration values; can be integrated in the display driver.

Control Interface. Provides the interface between the host processor and the display driver; can be integrated in the display driver.

Display Driving Circuit. As a part of display driver, used to convert timing signals and voltages to signals appropriate to drive the display device.

Power Supply. Used to convert system voltages to levels usable by the display device and display driver; can be integrated in the display driver.

Video Stream Interface. Used to receive video image data and timing signals from the host processor.

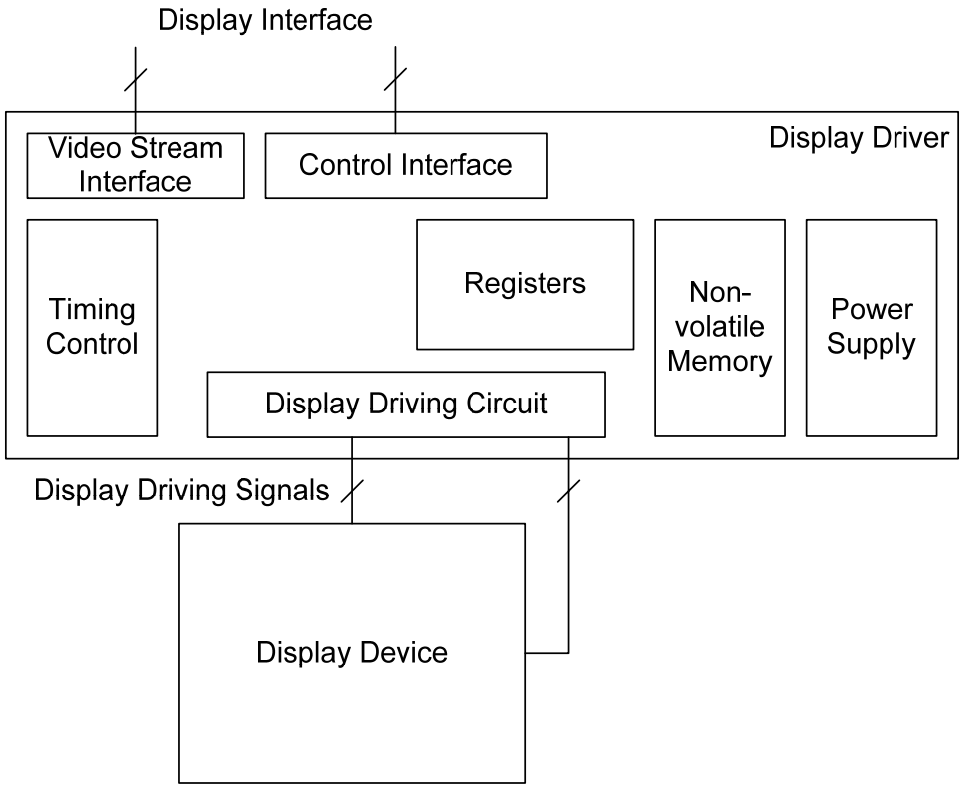


Figure 3 Type 3 Display Architecture Block Diagram

The Type 4 Display Architecture should consist of the following functional blocks

Display Device. Used to show image data.

Display Driver. May be one or more devices used to drive the display device.

Timing Controller. Provides timing signals to control the display device and display driver based on configuration information; can be integrated in the display driver.

Control Lines. Used to receive display behavior control information from the host processor.

Display Driving Circuit. As a part of display driver, used to convert timing signals and voltages to signals appropriate to drive the display device.

Power Supply. Used to convert system voltages to levels usable by the display device and display driver; can be integrated in the display driver.

Video Stream Interface. Used to receive video image data and timing signals from the host processor.

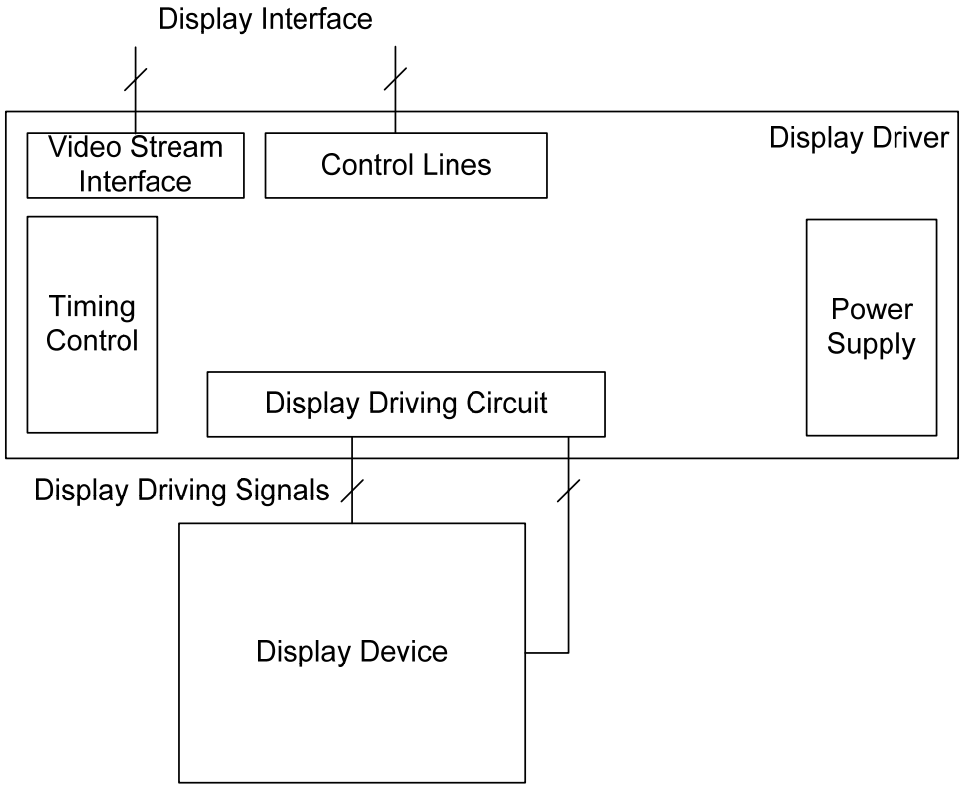


Figure 4 Type 4 Display Architecture Block Diagram

The power supply functional block should be controlled by the display driver for all applicable display architectures.

DPI-2 specifies the video stream interface for Type 2, 3 and 4 display architectures in a parallel implementation.

The control pins of the Type 4 display architecture shall be the control signals of DPI-2.

5 Display Pixel Interface Interoperability

There are two types of electrical connections between the host processor and the display module.

- Power Signals. Power is supplied from either the host processor or from a power management unit that is controlled by the host processor.
- Interface Signals. Pixel data, commands, and control information are transferred between the host processor and display module using the interface signals.

The host processor interface shall implement a 24-bit data width and accompanying control and timing signals, as specified in section 6. The host processor interface shall be capable of transferring data as 16-bit, 18-bit, or 24-bit words.

The display module interface shall be implemented with a 16-bit, 18-bit, or 24-bit data width.

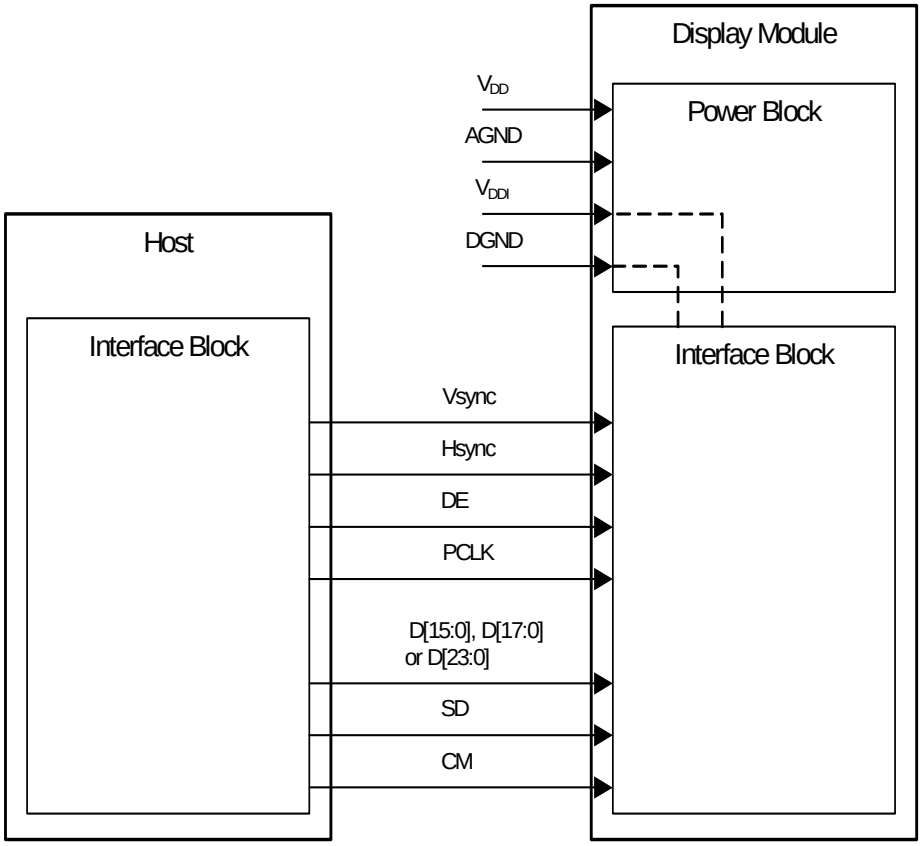


Figure 5 DPI Interface Signals and Power Connections

The host processor shall support all control signals for Type 2, Type 3, and Type 4 display architectures as shown in Figure 5. SD and CM are required control signals for Type 4 compliant display modules only.

Host processors shall support all timing parameter sets described in section 10. If a display module supports a display resolution in section 10 then it shall support the timing parameters as described for that resolution. Both the host processor and display module may operate over a range of values that include the given timing parameters.

249 Manufacturers shall document a DPI-2 device's parameter ranges for the parameters listed in section 10.

6 Interface Signal Description

6.1 Power Supply Connections

Table 1 Power supply connections

Symbol	Name	Description
V_{DD}	Power supply	Power supply for display module
V_{DDI}	I/F logic level supply	Logic level supply for interface signals
AGND	Power Ground	Analog GND for display-panel power supply
DGND	Logic level ground	Logic GND for logic functions on display panel

6.2 Interface Signals

Table 2 Interface Signals for DPI

Symbol	Name	I/O	Description
Vsync	Vertical sync	O	Vertical synchronization timing signal
Hsync	Horizontal sync	O	Horizontal synchronization timing signal
DE	Data enable	O	Data enable signal (assertion indicates valid pixels)
PCLK	Pixel Clock	O	Pixel clock for capturing pixels at display interface
D[15:0], D[17:0] or D[23:0]	Pixel Data	O	Pixel data in 16-bit, 18-bit, or 24-bit format
SD	Shutdown	O	Control pin to shut down display (used for Type 4 architecture only)
CM	Color Mode	O	Control pin for switching between normal color and reduced-color mode (used for Type 4 architecture only)

Note: I/O directions are defined from the host processor perspective

The host processor shall implement a 24-bit pixel-data bus width. The host processor interface can be configured for 16-bit or 18-bit data bus width.

The display module shall implement a 16-bit, 18-bit or 24-bit pixel-data bus width.

7 Programmable Timing Parameters

In normal operation, systems based on DPI architecture rely on the host processor to continuously provide complete frames of image data at a sufficient frame rate to avoid flicker or other visible artifacts.

The displayed image, or *frame*, is comprised of a rectangular array of pixels. The frame is transmitted from the host processor to a display module as a sequence of pixels, with each horizontal line of the image data sent as a group of consecutive pixels.

Vsync indicates the beginning of each frame of the displayed image.

Hsync signals the beginning of each horizontal line of pixels.

Each pixel value (16-, 18-, or 24-bit data) is transferred from the host processor to the display module during one pixel period. The rising edge of PCLK is used by the display module to capture pixel data. Since PCLK runs continuously, control signal DE is required to indicate when valid pixel data is being transmitted on the pixel data signals.

Figure 6 defines timing parameters for DPI operation.

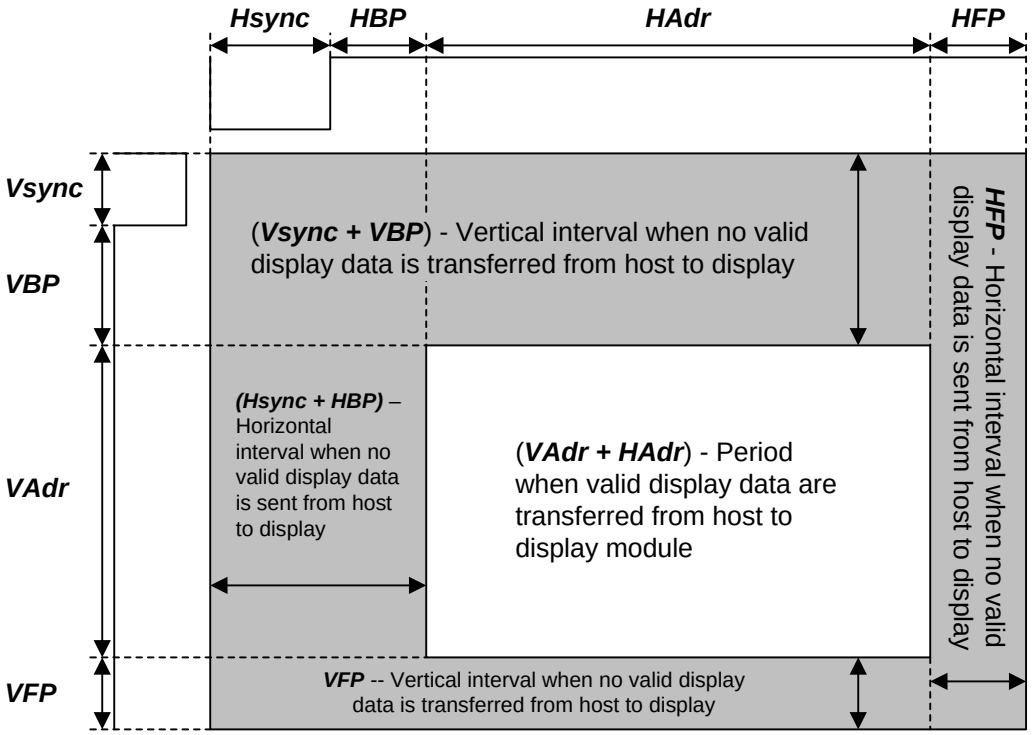


Figure 6 DPI Timing Parameters

Table 3 specifies requirements for DPI timing parameters. The host processor shall support the range specified in this table.

276 **Table 3 DPI Programmable Parameters**

Parameters	Symbols	Conditions	Min.	Step	Max.	Unit
Horizontal Synchronization	Hsync		1	1	-	PCLKCYC
Horizontal Back Porch	HBP		1	1	-	PCLKCYC
Horizontal Address	HAdr		176	1	800	PCLKCYC
Horizontal Front Porch	HFP		1	1	-	PCLKCYC
Vertical Synchronization	Vsync		1	1	-	Line
Vertical Back Porch	VBP		1	1	-	Line
Vertical Address	VAdr		208	1	480	Line
Vertical Front Porch	VFP		1	1	-	Line

277 Notes

278 1. Vertical period (one frame) shall be equal to the sum of Vsync + VBP + VAdr + VFP.

279 2. Horizontal period (one line) shall be equal to the sum of Hsync + HBP + HAdr + HFP.

280 3. Control signals PCLK and Hsync shall be transmitted as specified at all times while valid pixels
281 are transferred between the host processor and the display module.

8 Interface Color Coding

Table 4 specifies the mapping of data bits, as components of primary pixel color values R, G, and B, to signal lines at the interface. Host processors shall implement all color-coding configurations in Table 4. Peripherals shall implement one or more of the configurations in Table 4.

Table 4 Interface Color Coding

Signal Line	16-bit			18-bit		24-bit
	Configuration 1	Configuration 2	Configuration 3	Configuration 1	Configuration 2	
D23	(not used)	(not used)	(not used)	(not used)	(not used)	R7
D22	(not used)	(not used)	(not used)	(not used)	(not used)	R6
D21	(not used)	(not used)	R4	(not used)	R5	R5
D20	(not used)	R4	R3	(not used)	R4	R4
D19	(not used)	R3	R2	(not used)	R3	R3
D18	(not used)	R2	R1	(not used)	R2	R2
D17	(not used)	R1	R0	R5	R1	R1
D16	(not used)	R0	(not used)	R4	R0	R0
D15	R4	(not used)	(not used)	R3	(not used)	G7
D14	R3	(not used)	(not used)	R2	(not used)	G6
D13	R2	G5	G5	R1	G5	G5
D12	R1	G4	G4	R0	G4	G4
D11	R0	G3	G3	G5	G3	G3
D10	G5	G2	G2	G4	G2	G2
D9	G4	G1	G1	G3	G1	G1
D8	G3	G0	G0	G2	G0	G0
D7	G2	(not used)	(not used)	G1	(not used)	B7
D6	G1	(not used)	(not used)	G0	(not used)	B6
D5	G0	(not used)	B4	B5	B5	B5

Signal Line	16-bit			18-bit		24-bit
	Configuration 1	Configuration 2	Configuration 3	Configuration 1	Configuration 2	
D4	B4	B4	B3	B4	B4	B4
D3	B3	B3	B2	B3	B3	B3
D2	B2	B2	B1	B2	B2	B2
D1	B1	B1	B0	B1	B1	B1
D0	B0	B0	(not used)	B0	B0	B0

There are three mappings for 16-bit pixels to data signals, two mappings for 18-bit pixels to data signals, and one mapping for 24-bit pixels to data signals.

Notes:

1. Pixel values are specified as triplets for primary color components R, G, and B: R = Red, G = Green, B = Blue. R0 is the LSB for the red component, G0 is LSB for the green component, etc.

2. For 16-bit pixels, R primary color MSB is R4, R primary color LSB is R0; G primary color MSB is G5, G primary color LSB is G0; B primary color MSB is B4 and B primary color LSB is B0.

3. For 18-bit pixels, R primary color MSB is R5, R primary color LSB is R0; G primary color MSB is G5, G primary color LSB is G0; B primary color MSB is B5 and B primary color LSB is B0.

4. For 24-bit pixels, R primary color MSB is R7, R primary color LSB is R0; G primary color MSB is G7, G primary color LSB is G0; B primary color MSB is B7 and B primary color LSB is B0.

9 Interface Electrical Characteristics

9.1 Electrical Characteristics

9.1.1 Absolute Maximum Ratings

Table 5 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply	V_{DD}	DOI (Depends on Implementation)	V
Logic Level Supply	V_{DDI}	DOI (Depends on Implementation)	V
Logic Signal Input Voltage	V_I	DOI (Depends on Implementation)	V
Logic Signal Output Voltage	V_O	DOI (Depends on Implementation)	V

9.1.2 DC Characteristics

Table 6 DC Characteristics

Parameter	Symbol	Condition	Specification			Unit
			min	typ	max	
Power Supply Voltage	V_{DD}	Operating Voltage		DOI		V
Logic High Level Input Voltage	V_{IH}		$0.7V_{DDI}$		V_{DDI}	V
Logic Low Level Input Voltage	V_{IL}		0.0		$0.3V_{DDI}$	V
Logic High Level Input Current	I_{IH}	Except D[15:0], D[17:0] or D[23:0]			10	µA
	I_{IHD}	D[15:0], D[17:0] or D[23:0]			10	µA
Logic Low Level Input Current	I_{IH}	Except D[15:0], D[17:0] or D[23:0]	-10			µA
	I_{IHD}	D[15:0], D[17:0] or D[23:0]	-10			µA

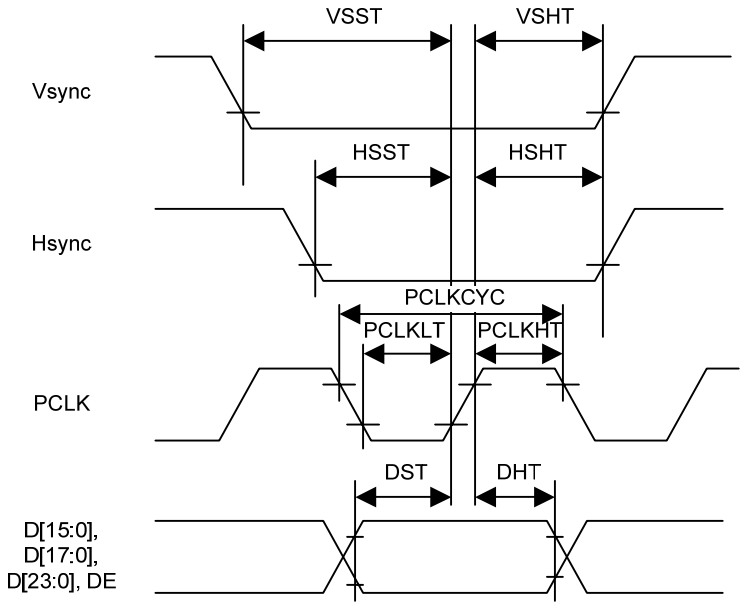
Note: Ta = -30 to 70 °C

305 **Table 7 Logic Level Supply Voltage Classification**

Parameter	Symbol	Class	Specification			Unit
			min	typ	max	
Logic Level Supply Voltage	V_{DDI}	1	1.1	1.2	1.3	V
		2	1.4	1.5	1.6	V
		3	1.7	1.8	1.9	V
		4	2.6	2.8	3.0	V

306 Note: Ta = -30 to 70 °C

307 ### 9.1.3 AC Characteristics



308

309 **Figure 7 DPI Signal Timings**

310 **Table 8 DPI-2 AC Characteristics**

Parameters	Symbols	Condition	Min.	Max.	Unit
Vsync Setup Time	VSST		T	-	ns
Vsync Hold Time	VSHT		T	-	ns
Hsync Setup Time	HSST		T	-	ns
Hsync Hold Time	HSHT		T	-	ns
Pixel Clock Duty Cycle		PCLKCYC	33	67	%

Parameters	Symbols	Condition	Min.	Max.	Unit
Pixel Clock Low Duration	PCLKLT		T	-	ns
Pixel Clock High Duration	PCLKHT		T	-	ns
Data Setup Time	DST		T	-	ns
Data Hold Time	DHT		T	-	ns

311 Note:

312 1. Ta = -30 to 70 °C, V_{DDI}=1.1V to 1.3V, 1.4V to 1.6V, 1.7V to 1.9V, 2.6V to 3.0V, GND=0V

313 2. Signal rise and fall times are not included in these values.

314 3. See Table 9 for T-values.

315 **Table 9 DPI-2 AC Characteristics, T-value**

Total Number of Pixels	Respresentative Display	T	Unit
Up to 38,720 pixels	176(H)x220(V)	40	ns
Up to 76,800 pixels	240(H)x320(V)	20	ns
Up to 307,200 pixels	640(H)x480(V)	10	ns
Up to 384,000 pixels	800(H)x480(V)	5	ns

10 DPI Timing Parameter Examples

Table 10 through Table 16 provides examples of DPI timing parameters for typical display module sizes.

Table 10 176 Horizontal x 208 Vertical Display Module

Parameters	Symbols	Conditions	Min.	Typ	Max.	Unit
PCLK Cycle	PCLKCYC			401		ns
Horizontal Synchronization	Hsync			2		PCLKCYC
Horizontal Back Porch	HBP			8		PCLKCYC
Horizontal Address	HAdr		-	176	-	PCLKCYC
Horizontal Front Porch	HFP			10		PCLKCYC
Vertical Synchronization	Vsync			2		Line
Vertical Back Porch	VBP			1		Line
Vertical Address	VAdr		-	208	-	Line
Vertical Front Porch	VFP			30		Line
Vsync Setup Time	VSST	See Table 8 and Table 9.				
Vsync Hold Time	VSHT					
Hsync Setup Time	HSST					
Hsync Hold Time	HSHT					
Data Setup Time	DST					
Data Hold Time	DHT					
Vertical Frequency(*)				60		Hz
Horizontal Frequency(*)				12.7		KHz
PCLK Frequency(*)				2.49		MHz

Note: * marked numbers are reference use only.

320 **Table 11 176 Horizontal x 220 Vertical Display Module**

Parameters	Symbols	Conditions	Min.	Typ	Max.	Unit
PCLK Cycle	PCLKCYC			379		ns
Horizontal Synchronization	Hsync			2		PCLKCYC
Horizontal Back Porch	HBP			8		PCLKCYC
Horizontal Address	HAdr		-	176	-	PCLKCYC
Horizontal Front Porch	HFP			10		PCLKCYC
Vertical Synchronization	Vsync			2		Line
Vertical Back Porch	VBP			1		Line
Vertical Address	VAdr		-	220	-	Line
Vertical Front Porch	VFP			1		Line
Vsync Setup Time	VSST	See Table 8 and Table 9.				
Vsync Hold Time	VSHT					
Hsync Setup Time	HSST					
Hsync Hold Time	HSHT					
Data Setup Time	DST					
Data Hold Time	DHT					
Vertical Frequency(*)				60.1		Hz
Horizontal Frequency(*)				13.5		KHz
PCLK Frequency(*)				2.64		MHz

321 Note: * marked numbers are reference use only.

322 **Table 12 240 Horizontal x 320 Vertical Display Module**

Parameters	Symbols	Conditions	Min.	Typ	Max.	Unit
PCLK Cycle	PCLKCYC			184		ns
Horizontal Synchronization	Hsync			10		PCLKCYC
Horizontal Back Porch	HBP			20		PCLKCYC
Horizontal Address	HAdr		-	240	-	PCLKCYC
Horizontal Front Porch	HFP			10		PCLKCYC
Vertical Synchronization	Vsync			2		Line
Vertical Back Porch	VBP			2		Line
Vertical Address	VAdr		-	320	-	Line
Vertical Front Porch	VFP			2		Line
Vsync Setup Time	VSST	See Table 8 and Table 9.				
Vsync Hold Time	VSHT					
Hsync Setup Time	HSST					
Hsync Hold Time	HSHT					
Data Setup Time	DST					
Data Hold Time	DHT					
Vertical Frequency(*)				59.6		Hz
Horizontal Frequency(*)				19.43		KHz
PCLK Frequency(*)				5.44		MHz

323 Note: * marked numbers are reference use only.

324 **Table 13 320 Horizontal x 240 Vertical Display Module**

Parameters	Symbols	Conditions	Min.	Typ	Max.	Unit
PCLK Cycle	PCLKCYC			172		ns
Horizontal Synchronization	Hsync			10		PCLKCYC
Horizontal Back Porch	HBP			20		PCLKCYC
Horizontal Address	HAdr		-	320	-	PCLKCYC
Horizontal Front Porch	HFP			40		PCLKCYC
Vertical Synchronization	Vsync			2		Line
Vertical Back Porch	VBP			2		Line
Vertical Address	VAdr		-	240	-	Line
Vertical Front Porch	VFP			4		Line
Vsync Setup Time	VSST	See Table 8 and Table 9.				
Vsync Hold Time	VSHT					
Hsync Setup Time	HSST					
Hsync Hold Time	HSHT					
Data Setup Time	DST					
Data Hold Time	DHT					
Vertical Frequency(*)				60		Hz
Horizontal Frequency(*)				14.9		KHz
PCLK Frequency(*)				5.8		MHz

325 Note: * marked numbers are reference use only.

326 **Table 14 480 Horizontal x 640 Vertical Display Module**

Parameters	Symbols	Conditions	Min.	Typ	Max.	Unit
PCLK Cycle	PCLKCYC			50		ns
Horizontal Synchronization	Hsync			8		PCLKCYC
Horizontal Back Porch	HBP			8		PCLKCYC
Horizontal Address	HAdr		-	480	-	PCLKCYC
Horizontal Front Porch	HFP			24		PCLKCYC
Vertical Synchronization	Vsync			2		Line
Vertical Back Porch	VBP			2		Line
Vertical Address	VAdr		-	640	-	Line
Vertical Front Porch	VFP			4		Line
Vsync Setup Time	VSST	See Table 8 and Table 9.				
Vsync Hold Time	VSHT					
Hsync Setup Time	HSST					
Hsync Hold Time	HSHT					
Data Setup Time	DST					
Data Hold Time	DHT					
Vertical Frequency(*)				59.4		Hz
Horizontal Frequency(*)				38.5		KHz
PCLK Frequency(*)				20		MHz

327 Note: * marked numbers are reference use only.

328 **Table 15 640 Horizontal x 480 Vertical Display Module**

Parameters	Symbols	Conditions	Min.	Typ	Max.	Unit
PCLK Cycle	PCLKCYC			47.8		ns
Horizontal Synchronization	Hsync			8		PCLKCYC
Horizontal Back Porch	HBP			8		PCLKCYC
Horizontal Address	HAdr		-	640	-	PCLKCYC
Horizontal Front Porch	HFP			44		PCLKCYC
Vertical Synchronization	Vsync			2		Line
Vertical Back Porch	VBP			2		Line
Vertical Address	VAdr		-	480	-	Line
Vertical Front Porch	VFP			4		Line
Vsync Setup Time	VSST	See Table 8 and Table 9.				
Vsync Hold Time	VSHT					
Hsync Setup Time	HSST					
Hsync Hold Time	HSHT					
Data Setup Time	DST					
Data Hold Time	DHT					
Vertical Frequency(*)				60		Hz
Horizontal Frequency(*)				29.3		KHz
PCLK Frequency(*)				21		MHz

329 Note: * marked numbers are reference use only.

330 **Table 16 800 Horizontal x 480 Vertical Display Module**

Parameters	Symbols	Conditions	Min.	Typ	Max.	Unit
PCLK Cycle	PCLKCYC			44.4		ns
Horizontal Synchronization	Hsync			10		PCLKCYC
Horizontal Back Porch	HBP			15		PCLKCYC
Horizontal Address	HAdr		-	800	-	PCLKCYC
Horizontal Front Porch	HFP			15		PCLKCYC
Vertical Synchronization	Vsync			2		Line
Vertical Back Porch	VBP			2		Line
Vertical Address	VAdr		-	480	-	Line
Vertical Front Porch	VFP			4		Line
Vsync Setup Time	VSST	See Table 8 and Table 9.				
Vsync Hold Time	VSHT					
Hsync Setup Time	HSST					
Hsync Hold Time	HSHT					
Data Setup Time	DST					
Data Hold Time	DHT					
Vertical Frequency(*)				55		Hz
Horizontal Frequency(*)				26.8		KHz
PCLK Frequency(*)				22.6		MHz

331 Note: * marked numbers are reference use only.

11 Type 2 and Type 3 Display Architecture Control Interfaces

The DBI Type C interface shall be used for Type 2 and Type 3 display architectures. See *MIPI Alliance Standard for Display Bus Interface* [2] for descriptions of the supported control interfaces.

12 Type 4 Architecture Shutdown and Color Mode Signals

12.1 Shutdown for Type 4 Architecture

The Shutdown signal, SD, is used to turn on or turn off the display module.

When SD is asserted high, the host processor should stop the video stream data to the display module to reduce interface signal power consumption. PCLK may also be turned off to further reduce power consumption.

The display module may reduce its power consumption by switching off its internal circuits. The control interface shall remain powered on.

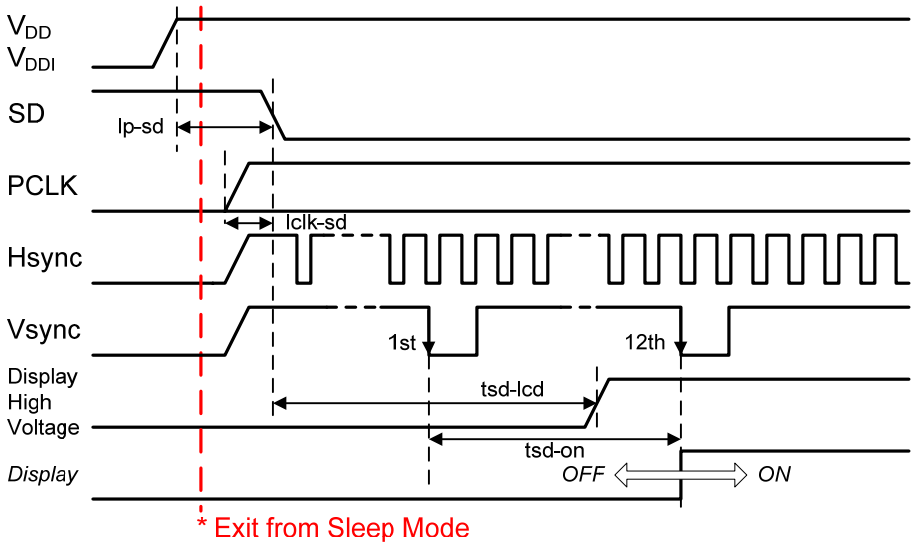
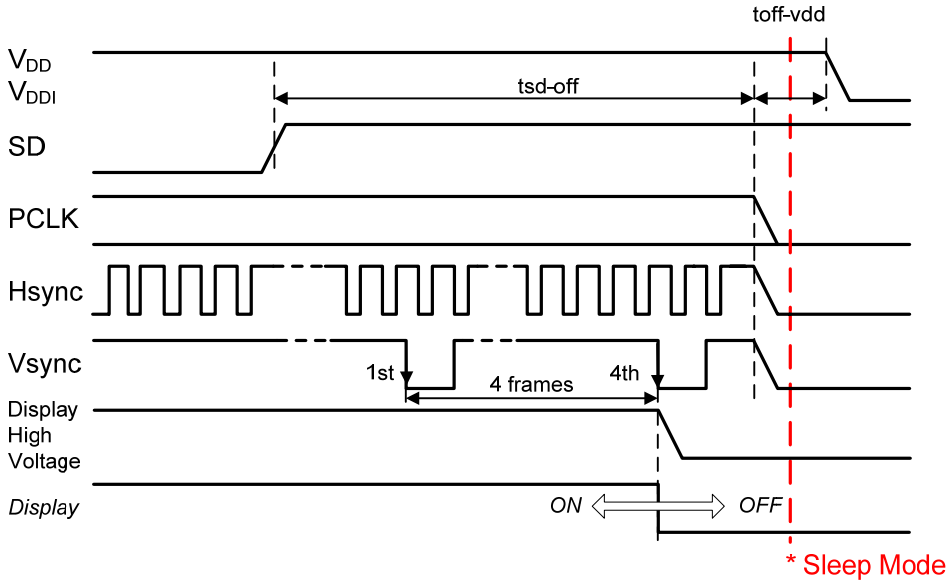


Figure 8 Power-on and Shutdown Recovery Sequence

Table 17 AC timing for power-on sequence and recovery sequence from shutdown

Parameters	Symbols	Condition	Min.	Typ.	Max.	Unit
V_{DD}/V_{DDI} – on to falling edge of SD	tp-sd		1	-	-	ms
PCLK input to the falling edge of SD	tclk-sd		1	-	-	PCLKCYC
Falling edge of SD to display start	tsd-on		-	12	-	Vertical period



346

347 **Figure 9 Power-off and Shutdown Sequence**

348 **Table 18 AC Timing for power-off sequence and shutdown sequence**

Parameters	Symbols	Condition	Min.	Typ.	Max.	Unit
Rising edge of SD to display off	tsd-off		4	-	-	Vertical period
Input-signal-off to V_{DD}/V_{DDI} off	toff-vdd		0	-	-	µs

349

12.2 Color Mode for Type 4 Architecture

The Color Mode signal, CM, is used to change the displayed number of colors.

When CM is asserted high, the display module shall show the image data using eight colors, MSB for each R, G, and B color components. All unnecessary circuits on the display module may be stopped at the same time to reduce display module power consumption.

The color mode change sequences are shown in Figure 10 and Figure 11.

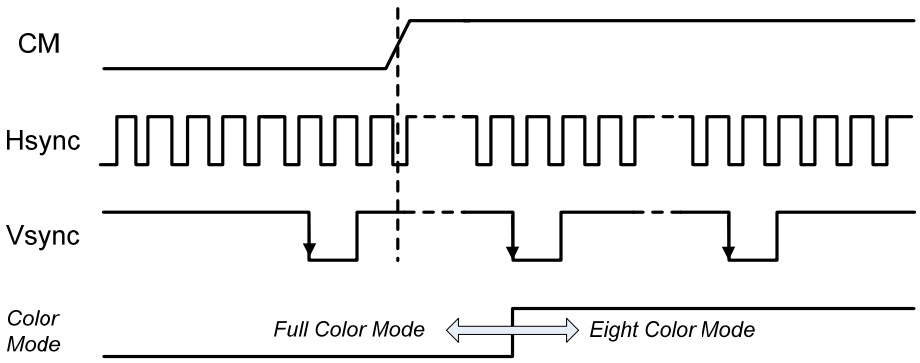


Figure 10 Full-color to 8-color Mode Transition Sequence

Transition from full-color mode to 8-color mode shall occur on the Vsync following a low-to-high transition on CM.

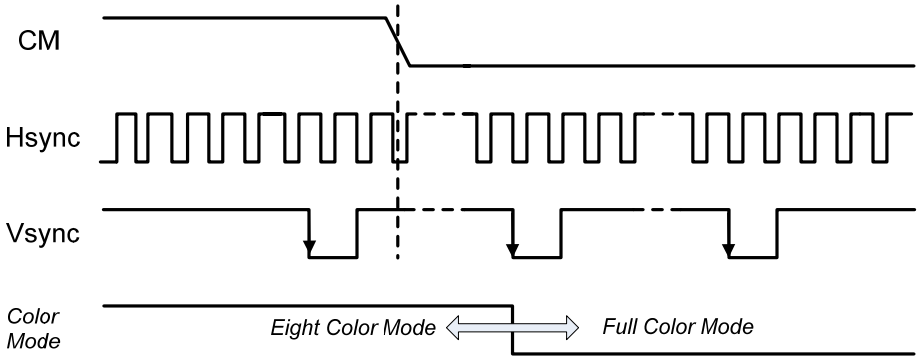


Figure 11 8-color to Full-color Mode Transition Sequence

Transition from 8-color mode to full-color mode shall occur on the Vsync following a high-to-low transition on CM.

13 Command Set

A host processor shall implement all commands specified in *MIPI Alliance Standard for Display Command Set* [1].

A display module shall implement the commands specific to the display architecture, Type 2 or Type 3, as defined in *MIPI Alliance Standard for Display Command Set* [1].