



# MIPI Alliance Specification for Display Serial Interface

**Version 1.02.00 – 28 June 2010**

MIPI Board Approved 20-Oct-2010

Further technical changes to this document are expected as work continues in the Display Working Group

**1 NOTICE OF DISCLAIMER**

2 The material contained herein is not a license, either expressly or impliedly, to any IPR owned or controlled  
3 by any of the authors or developers of this material or MIPI®. The material contained herein is provided on  
4 an "AS IS" basis and to the maximum extent permitted by applicable law, this material is provided AS IS  
5 AND WITH ALL FAULTS, and the authors and developers of this material and MIPI hereby disclaim all  
6 other warranties and conditions, either express, implied or statutory, including, but not limited to, any (if  
7 any) implied warranties, duties or conditions of merchantability, of fitness for a particular purpose, of  
8 accuracy or completeness of responses, of results, of workmanlike effort, of lack of viruses, and of lack of  
9 negligence.

10 All materials contained herein are protected by copyright laws, and may not be reproduced, republished,  
11 distributed, transmitted, displayed, broadcast or otherwise exploited in any manner without the express  
12 prior written permission of MIPI Alliance. MIPI, MIPI Alliance and the dotted rainbow arch and all related  
13 trademarks, tradenames, and other intellectual property are the exclusive property of MIPI Alliance and  
14 cannot be used without its express prior written permission.

15 ALSO, THERE IS NO WARRANTY OF CONDITION OF TITLE, QUIET ENJOYMENT, QUIET  
16 POSSESSION, CORRESPONDENCE TO DESCRIPTION OR NON-INFRINGEMENT WITH REGARD  
17 TO THIS MATERIAL OR THE CONTENTS OF THIS DOCUMENT. IN NO EVENT WILL ANY  
18 AUTHOR OR DEVELOPER OF THIS MATERIAL OR THE CONTENTS OF THIS DOCUMENT OR  
19 MIPI BE LIABLE TO ANY OTHER PARTY FOR THE COST OF PROCURING SUBSTITUTE  
20 GOODS OR SERVICES, LOST PROFITS, LOSS OF USE, LOSS OF DATA, OR ANY INCIDENTAL,  
21 CONSEQUENTIAL, DIRECT, INDIRECT, OR SPECIAL DAMAGES WHETHER UNDER  
22 CONTRACT, TORT, WARRANTY, OR OTHERWISE, ARISING IN ANY WAY OUT OF THIS OR  
23 ANY OTHER AGREEMENT, SPECIFICATION OR DOCUMENT RELATING TO THIS MATERIAL,  
24 WHETHER OR NOT SUCH PARTY HAD ADVANCE NOTICE OF THE POSSIBILITY OF SUCH  
25 DAMAGES.

26 Without limiting the generality of this Disclaimer stated above, the user of the contents of this Document is  
27 further notified that MIPI: (a) does not evaluate, test or verify the accuracy, soundness or credibility of the  
28 contents of this Document; (b) does not monitor or enforce compliance with the contents of this Document;  
29 and (c) does not certify, test, or in any manner investigate products or services or any claims of compliance  
30 with the contents of this Document. The use or implementation of the contents of this Document may  
31 involve or require the use of intellectual property rights ("IPR") including (but not limited to) patents,  
32 patent applications, or copyrights owned by one or more parties, whether or not Members of MIPI. MIPI  
33 does not make any search or investigation for IPR, nor does MIPI require or request the disclosure of any  
34 IPR or claims of IPR as respects the contents of this Document or otherwise.

35 Questions pertaining to this document, or the terms or conditions of its provision, should be addressed to:

36 MIPI Alliance, Inc.  
37 c/o IEEE-ISTO  
38 445 Hoes Lane  
39 Piscataway, NJ 08854  
40 Attn: Board Secretary

41

42	<b>Contents</b>	
43	Version 1.02.00 – 28 June 2010 .....	i
44	1 Overview .....	10
45	1.1 Scope .....	10
46	1.2 Purpose .....	10
47	2 Terminology (informative) .....	11
48	2.1 Definitions .....	11
49	2.2 Abbreviations .....	12
50	2.3 Acronyms .....	12
51	3 References (informative) .....	15
52	3.1 Display Bus Interface Standard for Parallel Signaling (DBI-2) .....	15
53	3.2 Display Pixel Interface Standard for Parallel Signaling (DPI-2) .....	16
54	3.3 MIPI Alliance Specification for Display Command Set (DCS) .....	16
55	3.4 MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) .....	16
56	3.5 MIPI Alliance Specification for D-PHY (D-PHY) .....	16
57	4 DSI Introduction .....	17
58	4.1 DSI Layer Definitions .....	18
59	4.2 Command and Video Modes .....	19
60	4.2.1 Command Mode .....	19
61	4.2.2 Video Mode Operation .....	19
62	4.2.3 Virtual Channel Capability .....	20
63	5 DSI Physical Layer .....	21
64	5.1 Data Flow Control .....	21
65	5.2 Bidirectionality and Low Power Signaling Policy .....	21
66	5.3 Command Mode Interfaces .....	22
67	5.4 Video Mode Interfaces .....	22
68	5.5 Bidirectional Control Mechanism .....	22
69	5.6 Clock Management .....	23
70	5.6.1 Clock Requirements .....	23
71	5.6.2 Clock Power and Timing .....	24
72	5.7 System Power-Up and Initialization .....	24
73	6 Multi-Lane Distribution and Merging .....	26
74	6.1 Multi-Lane Interoperability and Lane-number Mismatch .....	27
75	6.1.1 Clock Considerations with Multi-Lane .....	28
76	6.1.2 Bidirectionality and Multi-Lane Capability .....	28
77	6.1.3 SoT and EoT in Multi-Lane Configurations .....	28

78	7	Low-Level Protocol Errors and Contention .....	31
79	7.1	Low-Level Protocol Errors .....	31
80	7.1.1	SoT Error .....	31
81	7.1.2	SoT Sync Error .....	32
82	7.1.3	EoT Sync Error .....	32
83	7.1.4	Escape Mode Entry Command Error .....	33
84	7.1.5	LP Transmission Sync Error .....	33
85	7.1.6	False Control Error .....	33
86	7.2	Contention Detection and Recovery .....	34
87	7.2.1	Contention Detection in LP Mode .....	34
88	7.2.2	Contention Recovery Using Timers .....	34
89	7.3	Additional Timers .....	37
90	7.3.1	Turnaround Acknowledge Timeout (TA_TO) .....	37
91	7.3.2	Peripheral Reset Timeout (PR_TO) .....	37
92	7.4	Acknowledge and Error Reporting Mechanism .....	38
93	8	DSI Protocol .....	39
94	8.1	Multiple Packets per Transmission .....	39
95	8.2	Packet Composition .....	40
96	8.3	Endian Policy .....	41
97	8.4	General Packet Structure .....	41
98	8.4.1	Long Packet Format .....	41
99	8.4.2	Short Packet Format .....	43
100	8.5	Common Packet Elements .....	43
101	8.5.1	Data Identifier Byte .....	43
102	8.5.2	Error Correction Code .....	44
103	8.6	Interleaved Data Streams .....	45
104	8.6.1	Interleaved Data Streams and Bidirectionality .....	45
105	8.7	Processor to Peripheral Direction (Processor-Sourced) Packet Data Types .....	46
106	8.8	Processor-to-Peripheral Transactions – Detailed Format Description .....	47
107	8.8.1	Sync Event (H Start, H End, V Start, V End), Data Type = XX 0001 (0xX1) .....	47
108	8.8.2	EoTp, Data Type = 00 1000 (0x08) .....	47
109	8.8.3	Color Mode Off Command, Data Type = 00 0010 (0x02) .....	48
110	8.8.4	Color Mode On Command, Data Type = 01 0010 (0x12) .....	48
111	8.8.5	Shutdown Peripheral Command, Data Type = 10 0010 (0x22) .....	49
112	8.8.6	Turn On Peripheral Command, Data Type = 11 0010 (0x32) .....	49
113	8.8.7	Generic Short WRITE Packet with 0, 1, or 2 parameters, Data Types = 00 0011 (0x03), 01	
114		0011 (0x13), 10 0011 (0x23), Respectively .....	49

115	8.8.8	Generic READ Request with 0, 1, or 2 Parameters, Data Types = 00 0100 (0x04), 01 0100 (0x14), 10 0100(0x24), Respectively .....	49
117	8.8.9	DCS Commands .....	50
118	8.8.10	Set Maximum Return Packet Size, Data Type = 11 0111 (0x37).....	51
119	8.8.11	Null Packet (Long), Data Type = 00 1001 (0x09).....	51
120	8.8.12	Blanking Packet (Long), Data Type = 01 1001 (0x19).....	51
121	8.8.13	Generic Long Write, Data Type = 10 1001 (0x29).....	51
122	8.8.14	Loosely Packed Pixel Stream, 20-bit YCbCr 4:2:2 Format, Data Type = 00 1100 (0x0C).....	51
123	8.8.15	Packed Pixel Stream, 24-bit YCbCr 4:2:2 Format, Data Type = 01 1100 (0x1C).....	53
124	8.8.16	Packed Pixel Stream, 16-bit YCbCr 4:2:2 Format, Data Type = 10 1100 (0x2C).....	54
125	8.8.17	Packed Pixel Stream, 30-bit Format, Long Packet, Data Type = 00 1101 (0x0D) .....	54
126	8.8.18	Packed Pixel Stream, 36-bit Format, Long Packet, Data Type = 01 1101 (0x1D) .....	55
127	8.8.19	Packed Pixel Stream, 12-bit YCbCr 4:2:0 Format, Data Type = 11 1101 (0x3D) .....	56
128	8.8.20	Packed Pixel Stream, 16-bit Format, Long Packet, Data Type 00 1110 (0x0E).....	57
129	8.8.21	Packed Pixel Stream, 18-bit Format, Long Packet, Data Type = 01 1110 (0x1E).....	58
130	8.8.22	Pixel Stream, 18-bit Format in Three Bytes, Long Packet, Data Type = 10 1110 (0x2E).....	60
131	8.8.23	Packed Pixel Stream, 24-bit Format, Long Packet, Data Type = 11 1110 (0x3E).....	61
132	8.8.24	DO NOT USE and Reserved Data Types .....	62
133	8.9	Peripheral-to-Processor (Reverse Direction) LP Transmissions .....	62
134	8.9.1	Packet Structure for Peripheral-to-Processor LP Transmissions .....	62
135	8.9.2	System Requirements for ECC and Checksum and Packet Format.....	63
136	8.9.3	Appropriate Responses to Commands and ACK Requests.....	63
137	8.9.4	Format of Acknowledge and Error Report and Read Response Data Types .....	65
138	8.9.5	Error Reporting Format .....	65
139	8.10	Peripheral-to-Processor Transactions – Detailed Format Description.....	67
140	8.10.1	Acknowledge and Error Report, Data Type 00 0010 (0x02) .....	68
141	8.10.2	Generic Short Read Response, 1 or 2 Bytes, Data Types = 01 0001 or 01 0010, Respectively	68
142		68	
143	8.10.3	Generic Long Read Response with Optional Checksum, Data Type = 01 1010 (0x1A).....	68
144	8.10.4	DCS Long Read Response with Optional Checksum, Data Type 01 1100 (0x1C) .....	69
145	8.10.5	DCS Short Read Response, 1 or 2 Bytes, Data Types = 10 0001 or 10 0010, Respectively .	69
146	8.10.6	Multiple Transmissions and Error Reporting .....	69
147	8.10.7	Clearing Error Bits.....	69
148	8.11	Video Mode Interface Timing .....	69
149	8.11.1	Transmission Packet Sequences .....	70
150	8.11.2	Non-Burst Mode with Sync Pulses .....	71
151	8.11.3	Non-Burst Mode with Sync Events .....	72
152	8.11.4	Burst Mode .....	73

153 8.11.5 Parameters .....74

154 8.12 TE Signaling in DSI .....75

155 9 Error-Correcting Code (ECC) and Checksum .....77

156 9.1 Packet Header Error Detection/Correction .....77

157 9.2 Hamming Code Theory .....77

158 9.3 Hamming-modified Code Applied to DSI Packet Headers .....78

159 9.4 ECC Generation on the Transmitter .....81

160 9.5 Applying ECC on the Receiver .....82

161 9.6 Checksum Generation for Long Packet Payloads.....82

162 10 Compliance, Interoperability, and Optional Capabilities .....84

163 10.1 Display Resolutions.....84

164 10.2 Pixel Formats.....85

165 10.2.1 Video Mode .....85

166 10.2.2 Command Mode .....85

167 10.3 Number of Lanes .....85

168 10.4 Maximum Lane Frequency.....85

169 10.5 Bidirectional Communication.....86

170 10.6 ECC and Checksum Capabilities.....86

171 10.7 Display Architecture.....86

172 10.8 Multiple Peripheral Support .....86

173 10.9 EoTp Support and Interoperability .....86

174 Annex A Contention Detection and Recovery Mechanisms (informative).....87

175 A.1 PHY Detected Contention .....87

176 A.1.1 Protocol Response to PHY Detected Faults.....87

177 Annex B Checksum Generation Example (informative) .....93

178 Annex C Interlaced Video Transmission Sourcing.....95

179

180

181	<b>Figures</b>	
182	Figure 1 DSI Transmitter and Receiver Interface.....	17
183	Figure 2 DSI Layers .....	18
184	Figure 3 Basic HS Transmission Structure.....	21
185	Figure 4 Peripheral Power-Up Sequencing Example .....	25
186	Figure 5 Lane Distributor Conceptual Overview .....	26
187	Figure 6 Lane Merger Conceptual Overview .....	27
188	Figure 7 Four-Lane Transmitter with Two-Lane Receiver Example .....	28
189	Figure 8 Two Lane HS Transmission Example.....	29
190	Figure 9 Three Lane HS Transmission Example.....	30
191	Figure 10 HS Transmission Examples with EoTp disabled .....	40
192	Figure 11 HS Transmission Examples with EoTp enabled .....	40
193	Figure 12 Endian Example (Long Packet).....	41
194	Figure 13 Long Packet Structure.....	42
195	Figure 14 Short Packet Structure.....	43
196	Figure 15 Data Identifier Byte.....	44
197	Figure 16 Interleaved Data Stream Example with EoTp disabled.....	45
198	Figure 17 Logical Channel Block Diagram (Receiver Case) .....	45
199	Figure 18 20-bit per Pixel – YCbCr 4:2:2 Format, Long Packet.....	52
200	Figure 19 24-bit per Pixel – YCbCr 4:2:2 Format, Long Packet.....	53
201	Figure 20 16-bit per Pixel – YCbCr 4:2:2 Format, Long Packet.....	54
202	Figure 21 30-bit per Pixel (Packed) – RGB Color Format, Long Packet .....	55
203	Figure 22 36-bit per Pixel (Packed) – RGB Color Format, Long Packet .....	56
204	Figure 23 12-bit per Pixel – YCbCr 4:2:0 Format (Odd Line), Long Packet .....	57
205	Figure 24 12-bit per Pixel – YCbCr 4:2:0 Format (Even Line), Long Packet.....	57
206	Figure 25 16-bit per Pixel – RGB Color Format, Long Packet .....	58
207	Figure 26 18-bit per Pixel (Packed) – RGB Color Format, Long Packet .....	59
208	Figure 27 18-bit per Pixel (Loosely Packed) – RGB Color Format, Long Packet .....	60
209	Figure 28 24-bit per Pixel – RGB Color Format, Long Packet .....	61
210	Figure 29 Video Mode Interface Timing Legend.....	71
211	Figure 30 Video Mode Interface Timing: Non-Burst Transmission with Sync Start and End.....	72
212	Figure 31 Video Mode Interface Timing: Non-burst Transmission with Sync Events .....	73
213	Figure 32 Video Mode Interface Timing: Burst Transmission.....	74
214	Figure 33 24-bit ECC generation on TX side .....	81
215	Figure 34 24-bit ECC on RX Side Including Error Correction .....	82
216	Figure 35 Checksum Transmission .....	83

217 Figure 36 16-bit CRC Generation Using a Shift Register .....83  
218 Figure 37 LP High  $\leftrightarrow$  LP Low Contention Case 1 .....89  
219 Figure 38 LP High  $\leftrightarrow$  LP Low Contention Case 2 .....91  
220 Figure 39 LP High  $\leftrightarrow$  LP Low Contention Case 3 .....92  
221 Figure 40 Video Mode Interface Timing: Non-burst Transmission with Sync Start and End (Interlaced  
222 Video).....95  
223 Figure 41 Video Mode Interface Timing: Non-burst Transmission with Sync Events (Interlaced Video) ...96  
224  
225



226

**Tables**

227	Table 1 Sequence of Events to Resolve SoT Error (HS RX Side) .....	32
228	Table 2 Sequence of Events to Resolve SoT Sync Error (HS RX Side).....	32
229	Table 3 Sequence of Events to Resolve EoT Sync Error (HS RX Side) .....	33
230	Table 4 Sequence of Events to Resolve Escape Mode Entry Command Error (RX Side) .....	33
231	Table 5 Sequence of Events to Resolve LP Transmission Sync Error (RX Side) .....	33
232	Table 6 Sequence of Events to Resolve False Control Error (RX Side).....	34
233	Table 7 Low-Level Protocol Error Detection and Reporting .....	34
234	Table 8 Required Timers and Timeout Summary .....	35
235	Table 9 Sequence of Events for HS RX Timeout (Peripheral initially HS RX) .....	35
236	Table 10 Sequence of Events for HS TX Timeout (Host Processor initially HS TX).....	36
237	Table 11 Sequence of Events for LP TX-Peripheral Timeout (Peripheral initially LP TX).....	36
238	Table 12 Sequence of Events for Host Processor Wait Timeout (Peripheral initially TX) .....	36
239	Table 13 Sequence of Events for BTA Acknowledge Timeout (Peripheral initially TX).....	37
240	Table 14 Sequence of Events for BTA Acknowledge Timeout (Host Processor initially TX) .....	37
241	Table 15 Sequence of Events for Peripheral Reset Timeout .....	37
242	Table 16 Data Types for Processor-sourced Packets.....	46
243	Table 17 EoT Support for Host and Peripheral .....	48
244	Table 18 Error Report Bit Definitions .....	66
245	Table 19 Data Types for Peripheral-sourced Packets.....	67
246	Table 20 Required Peripheral Timing Parameters.....	74
247	Table 21 ECC Syndrome Association Matrix .....	78
248	Table 22 ECC Parity Generation Rules .....	79
249	Table 23 Display Resolutions.....	84
250	Table 24 LP High $\leftrightarrow$ LP Low Contention Case 1 .....	87
251	Table 25 LP High $\leftrightarrow$ LP Low Contention Case 2 .....	90
252	Table 26 LP High $\leftrightarrow$ LP Low Contention Case 3 .....	92

253

# 254 MIPI Alliance Specification for 255 Display Serial Interface

## 256 1 Overview

257 The Display Serial Interface Specification defines protocols between a host processor and peripheral  
258 devices that adhere to MIPI Alliance specifications for mobile device interfaces. The DSI specification  
259 builds on existing specifications by adopting pixel formats and command set defined in [MIPI02],  
260 [MIPI03], and [MIPI01].

### 261 1.1 Scope

262 Interface protocols as well as a description of signal timing relationships are within the scope of this  
263 document.

264 Electrical specifications and physical specifications are out of scope for this document. In addition, legacy  
265 interfaces such as DPI-2 and DBI-2 are also out of scope for this document. Furthermore, device usage of  
266 auxiliary buses such as I<sup>2</sup>C or SPI, while not precluded by this specification, are also not within its scope.

### 267 1.2 Purpose

268 The Display Serial Interface specification defines a high-speed serial interface between a peripheral, such  
269 as an active-matrix display module, and a host processor in a mobile device. By standardizing this  
270 interface, components may be developed that provide higher performance, lower power, less EMI and  
271 fewer pins than current devices, while maintaining compatibility across products from multiple vendors.  
272

## 273 2 Terminology (informative)

274 The MIPI Alliance has adopted Section 13.1 of the IEEE Standards Style Manual, which dictates use of the  
275 words “shall”, “should”, “may”, and “can” in the development of documentation, as follows:

276 The word *shall* is used to indicate mandatory requirements strictly to be followed in order  
277 to conform to the standard and from which no deviation is permitted (*shall equals is*  
278 *required to*).

279 The use of the word *must* is deprecated and shall not be used when stating mandatory  
280 requirements; *must* is used only to describe unavoidable situations.

281 The use of the word *will* is deprecated and shall not be used when stating mandatory  
282 requirements; *will* is only used in statements of fact.

283 The word *should* is used to indicate that among several possibilities one is recommended  
284 as particularly suitable, without mentioning or excluding others; or that a certain course  
285 of action is preferred but not necessarily required; or that (in the negative form) a certain  
286 course of action is deprecated but not prohibited (*should equals is recommended that*).

287 The word *may* is used to indicate a course of action permissible within the limits of the  
288 standard (*may equals is permitted*).

289 The word *can* is used for statements of possibility and capability, whether material,  
290 physical, or causal (*can equals is able to*).

291 All sections are normative, unless they are explicitly indicated to be informative.

292 Numbers are decimal unless otherwise indicated. Hexadecimal numbers have a “0x” prefix. Binary  
293 numbers are prefixed by “0b”.

### 294 2.1 Definitions

295 **Forward Direction:** The signal direction is defined relative to the direction of the high-speed serial clock.  
296 Transmission from the side sending the clock to the side receiving the clock is the forward direction.

297 **Half duplex:** Bidirectional data transmission over a Lane allowing both transmission and reception but  
298 only in one direction at a time.

299 **HS Transmission:** Sending one or more packets in the forward direction in HS Mode. A HS Transmission  
300 is delimited before and after packet transmission by LP-11 states.

301 **Host Processor:** Hardware and software that provides the core functionality of a mobile device.

302 **Lane:** Consists of two complementary Lane Modules communicating via two-line, point-to-point Lane  
303 Interconnects. A Lane can be used for either Data or Clock signal transmission.

304 **Lane Interconnect:** Two-line, point-to-point interconnect used for both differential high-speed signaling  
305 and low-power, single-ended signaling.

306 **Lane Module:** Module at each side of the Lane for driving and/or receiving signals on the Lane.

307 **Link:** A connection between two devices containing one Clock Lane and at least one Data Lane. A Link  
308 consists of two PHYs and two Lane Interconnects.

309 **LP Transmission:** Sending one or more packets in either direction in LP Mode or Escape Mode. A LP  
310 Transmission is delimited before and after packet transmission by LP-11 states.

311 **Packet:** A group of four or more bytes organized in a specified way to transfer data across the interface. All  
312 packets have a minimum specified set of components. The byte is the fundamental unit of data from which  
313 packets are made.

314 **Payload:** Application data only – with all Link synchronization, header, ECC and checksum and other  
315 protocol-related information removed. This is the “core” of transmissions between host processor and  
316 peripheral.

317 **PHY:** The set of Lane Modules on one side of a Link.

318 **PHY Configuration:** A set of Lanes that represent a possible Link. A PHY configuration consists of a  
319 minimum of two Lanes: one Clock Lane and one or more Data Lanes.

320 **Reverse Direction:** Reverse direction is the opposite of the forward direction. See the description for  
321 Forward Direction.

322 **Transmission:** Refers to either HS or LP Transmission. See the HS Transmission and LP Transmission  
323 definitions for descriptions of the different transmission modes.

324 **Virtual Channel:** Multiple independent data streams for up to four peripherals are supported by this  
325 specification. The data stream for each peripheral is a *Virtual Channel*. These data streams may be  
326 interleaved and sent as sequential packets, with each packet dedicated to a particular peripheral or channel.  
327 Packet protocol includes information that directs each packet to its intended peripheral.

328 **Word Count:** Number of bytes within the payload.

## 329 **2.2 Abbreviations**

330 e.g. For example

## 331 **2.3 Acronyms**

332	AIP	Application Independent Protocol
333	AM	Active matrix (display technology)
334	ASP	Application Specific Protocol
335	BLLP	Blanking or Low Power interval
336	BPP	Bits per Pixel
337	BTA	Bus Turn-Around
338	CSI	Camera Serial Interface
339	DBI	Display Bus Interface

340	DI	Data Identifier
341	DMA	Direct Memory Access
342	DPI	Display Pixel Interface
343	DSI	Display Serial Interface
344	DT	Data Type
345	ECC	Error-Correcting Code
346	EMI	Electro Magnetic interference
347	EoTp	End of Transmission Packet
348	ESD	Electrostatic Discharge
349	Fps	Frames per second
350	HBP	Horizontal Back Porch
351	HFP	Horizontal Front Porch
352	HS	High Speed
353	HSA	Horizontal Sync Active
354	HSE	Horizontal Sync End
355	HSS	Horizontal Sync Start
356	ISTO	Industry Standards and Technology Organization
357	LP	Low Power
358	LPS	Low Power State (state of serial data line when not transferring high-speed serial data)
359	LSB	Least Significant Bit
360	Mbps	Megabits per second
361	MIPI	Mobile Industry Processor Interface
362	MSB	Most Significant Bit
363	PF	Packet Footer
364	PH	Packet Header
365	PHY	Physical Layer
366	PPI	PHY-Protocol Interface

367	QCIF	Quarter-size CIF (resolution 176x144 pixels or 144x176 pixels)
368	QVGA	Quarter-size Video Graphics Array (resolution 320x240 pixels or 240x320 pixels)
369	RGB	Color presentation (Red, Green, Blue)
370	SLVS	Scalable Low Voltage Signaling
371	SoT	Start of Transmission
372	SVGA	Super Video Graphics Array (resolution 800x600 pixels or 600x800 pixels)
373	ULPS	Ultra-low Power State
374	VGA	Video Graphics Array (resolution 640x480 pixels or 480x640 pixels)
375	VSA	Vertical Sync Active
376	VSE	Vertical Sync End
377	VSS	Vertical Sync Start
378	WC	Word Count
379	WVGA	Wide VGA (resolution 800x480 pixels or 480x800 pixels)
380		

### 381 **3 References (informative)**

- 382 [MIPI01] *MIPI Alliance Specification for Display Command Set*, version 1.02.00, MIPI Alliance,  
383 Inc., 23 July 2009
- 384 [MIPI02] *MIPI Alliance Standard for Display Bus Interface (DBI-2)*, version 2.00, MIPI Alliance,  
385 Inc., 29 November 2005
- 386 [MIPI03] *MIPI Alliance Standard for Display Pixel Interface (DPI-2)*, version 2.00, MIPI Alliance,  
387 Inc., 15 September 2005
- 388 [MIPI04] *MIPI Alliance Specification for D-PHY*, version 1.00.00, MIPI Alliance, Inc., 14 May  
389 2009
- 390 [CEA01] CEA-861-E, *A DTV Profile for Uncompressed High Speed Digital Interfaces*,  
391 <[http://www.ce.org/Standards/browseByCommittee\\_2641.asp](http://www.ce.org/Standards/browseByCommittee_2641.asp)>, Consumer Electronics  
392 Association, March 2008
- 393 [ITU01] BT.601-6, *Studio encoding parameters of digital television for standard 4:3 and wide  
394 screen 16:9 aspect ratios*, <<http://www.itu.int/rec/R-REC-BT.601-6-200701-I/en>>,  
395 International Telecommunications Union, 23 February 2007
- 396 [ITU02] BT.709-5, *Parameter values for the HDTV standards for production and international  
397 programme exchange*, <<http://www.itu.int/rec/R-REC-BT.709-5-200204-I/en>>,  
398 International Telecommunications Union, 27 August 2009
- 399 [ITU03] BT.656-5, *Interface for digital component video signals in 525-line and 625-line  
400 television systems operating at the 4:2:2 level of Recommendation ITU-R BT.601*,  
401 <<http://www.itu.int/rec/R-REC-BT.656-5-200712-I/en>>, International  
402 Telecommunications Union, 1 January 2008
- 403 [SMPT01] EG 36-2000, *Transformations Between Television Component Color Signals*, Society for  
404 Motion Picture and Television Engineers, 23 March 2000

405 Much of DSI is based on existing MIPI Alliance specifications as well as several MIPI Alliance  
406 specifications in simultaneous development. In the Application Layer, DSI duplicates pixel formats used in  
407 [MIPI03] when it is in *Video Mode* operation. For display modules with a display controller and frame  
408 buffer, DSI shares a common command set with [MIPI02]. The command set is documented in [MIPI01].

#### 409 **3.1 Display Bus Interface Standard for Parallel Signaling (DBI-2)**

410 DBI-2 is a MIPI Alliance standard for parallel interfaces to display modules having display controllers and  
411 frame buffers. For systems based on these standards, the host processor loads images to the on-panel frame  
412 buffer through the display processor. Once loaded, the display controller manages all display refresh  
413 functions on the display module without further intervention from the host processor. Image updates  
414 require the host processor to write new data into the frame buffer.

415 DBI-2 specifies a parallel interface where data can be sent to the peripheral over an 8-, 9- or 16-bit-wide  
416 data bus, with additional control signals. DBI-2 supports a 1-bit data bus interface mode as well.

417 The DSI specification supports a Command Mode of operation. Like the parallel DBI, a DSI-compliant  
418 interface sends commands and parameters to the display. However, all information in DSI is first serialized  
419 before transmission to the display module. At the display, serial information is transformed back to parallel  
420 data and control signals for the on-panel display controller. Similarly, the display module can return status  
421 information and requested memory data to the host processor, using the same serial data path.

### 422 **3.2 Display Pixel Interface Standard for Parallel Signaling (DPI-2)**

423 DPI-2 is a MIPI Alliance standard for parallel interfaces to display modules without on-panel display  
424 controller or frame buffer. These display modules rely on a steady flow of pixel data from host processor to  
425 the display, to maintain an image without flicker or other visual artifacts. MIPI Alliance standards  
426 document several pixel formats for *Active Matrix* (AM) display modules.

427 Like DBI-2, DPI-2 is a MIPI Alliance standard for parallel interfaces. The data path may be 16-, 18-, or 24-  
428 bits wide, depending on pixel format(s) supported by the display module. This document refers to DPI  
429 mode of operation as Video Mode.

430 Some display modules that use Video Mode in normal operation also make use of a simplified form of  
431 Command Mode, when in low-power state. These display modules can shut down the streaming video  
432 interface and continue to refresh the screen from a small local frame buffer, at reduced resolution and pixel  
433 depth. The local frame buffer shall be loaded, prior to interface shutdown, with image content to be  
434 displayed when in low-power operation. These display modules can switch mode in response to power-  
435 control commands.

### 436 **3.3 MIPI Alliance Specification for Display Command Set (DCS)**

437 DCS is a MIPI Alliance specification for the command set used by DSI and DBI-2 standards. Commands  
438 are sent from the host processor to the display module. On the display module, a display controller receives  
439 and interprets commands, then takes appropriate action. Commands fall into four broad categories: read  
440 register, write register, read memory and write memory. A command may be accompanied by multiple  
441 parameters.

### 442 **3.4 MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2)**

443 CSI-2 is a MIPI Alliance standard for serial interface between a camera module and host processor. It is  
444 based on the same physical layer technology and low-level protocols as DSI. Some significant differences  
445 between DSI and CSI-2 are:

- 446 • CSI-2 uses unidirectional high-speed Link, whereas DSI is half-duplex bidirectional Link
- 447 • CSI-2 makes use of a secondary channel, based on I<sup>2</sup>C, for control and status functions

448 CSI-2 data direction is from peripheral (Camera Module) to host processor, while DSI's primary data  
449 direction is from host processor to peripheral (Display Module).

### 450 **3.5 MIPI Alliance Specification for D-PHY (D-PHY)**

451 [MIPI04] provides the physical layer definition for DSI. The functionality specified by the D-PHY  
452 specification covers all electrical and timing aspects, as well as low-level protocols, signaling, and message  
453 transmissions in various operating modes.

454

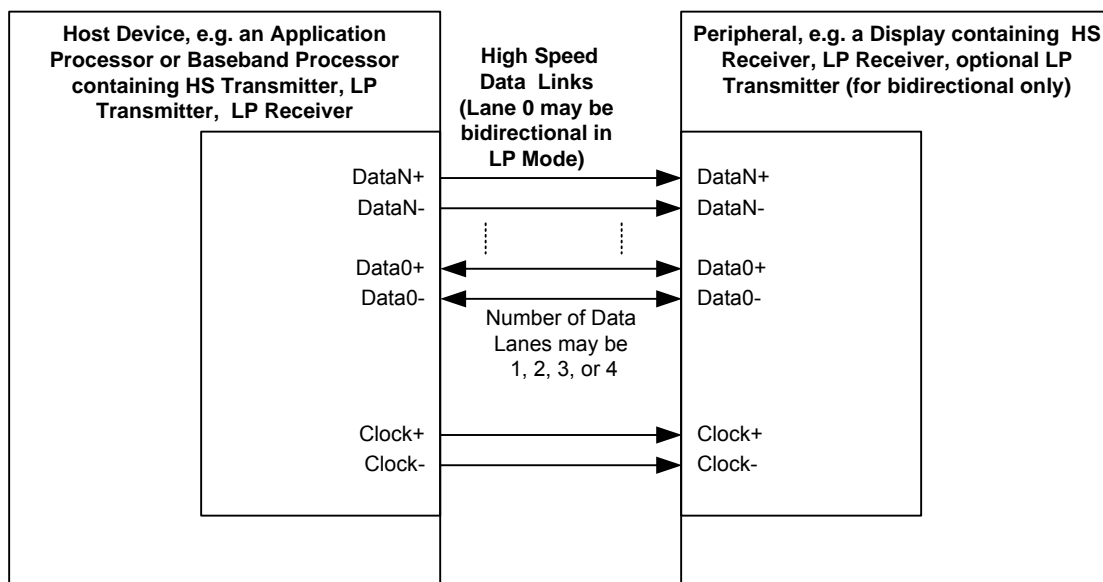


455 **4 DSI Introduction**

456 DSI specifies the interface between a host processor and a peripheral such as a display module. It builds on  
 457 existing MIPI Alliance specifications by adopting pixel formats and command set specified in DPI-2, DBI-  
 458 2 and DCS standards.

459 Figure 1 shows a simplified DSI interface. From a conceptual viewpoint, a DSI-compliant interface  
 460 performs the same functions as interfaces based on DBI-2 and DPI-2 standards or similar parallel display  
 461 interfaces. It sends pixels or commands to the peripheral, and can read back status or pixel information  
 462 from the peripheral. The main difference is that DSI serializes all pixel data, commands, and events that, in  
 463 traditional or legacy interfaces, are normally conveyed to and from the peripheral on a parallel data bus  
 464 with additional control signals.

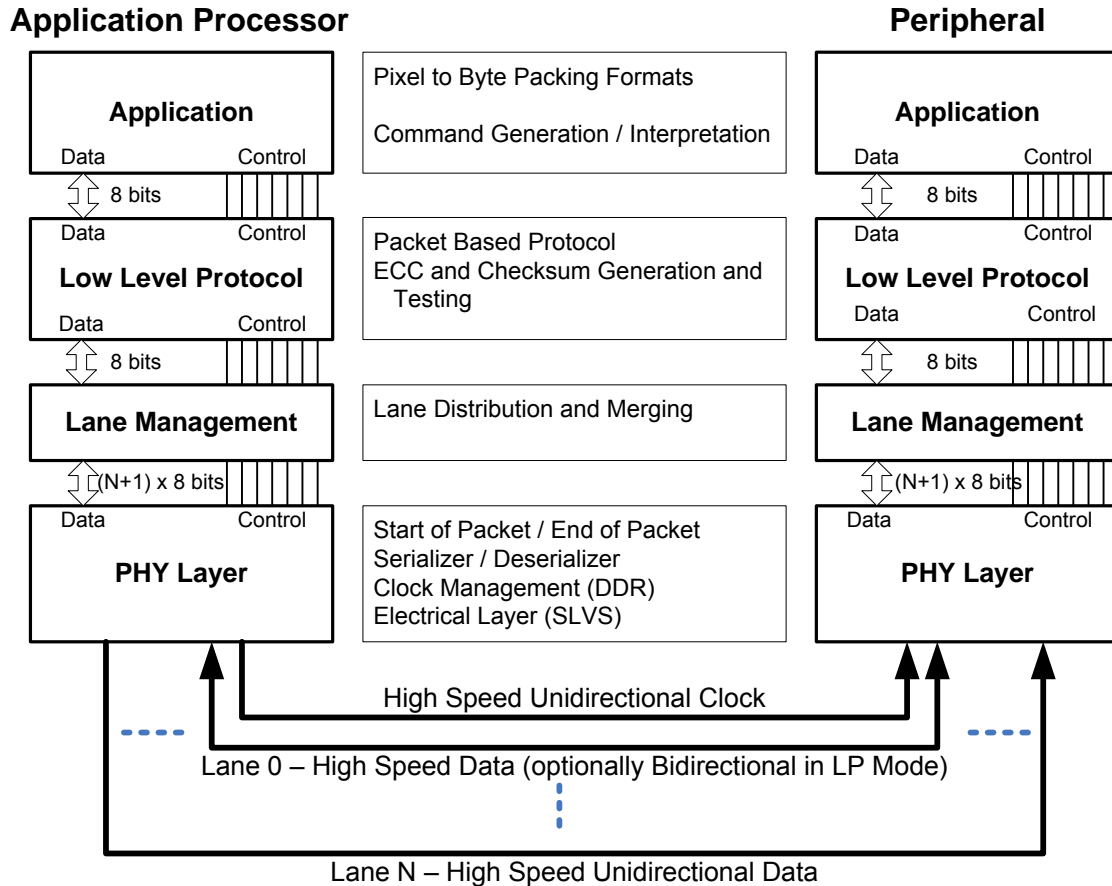
465 From a system or software point of view, the serialization and deserialization operations should be  
 466 transparent. The most visible, and unavoidable, consequence of transformation to serial data and back to  
 467 parallel is increased latency for transactions that require a response from the peripheral. For example,  
 468 reading a pixel from the frame buffer on a display module has a higher latency using DSI than DBI.  
 469 Another fundamental difference is the host processor's inability during a read transaction to throttle the  
 470 rate, or size, of returned data.



471

472

**Figure 1 DSI Transmitter and Receiver Interface**

473 **4.1 DSI Layer Definitions**

474

475

**Figure 2 DSI Layers**

476 A conceptual view of DSI organizes the interface into several functional layers. A description of the layers  
477 follows and is also shown in Figure 2.

478 **PHY Layer:** The *PHY Layer* specifies transmission medium (electrical conductors), the input/output  
479 circuitry and the clocking mechanism that captures “ones” and “zeroes” from the serial bit stream. This part  
480 of the specification documents the characteristics of the transmission medium, electrical parameters for  
481 signaling and the timing relationship between clock and Data Lanes.

482 The mechanism for signaling Start of Transmission (SoT) and End of Transmission (EoT) is specified, as  
483 well as other “out of band” information that can be conveyed between transmitting and receiving PHYs.  
484 Bit-level and byte-level synchronization mechanisms are included as part of the PHY. Note that the  
485 electrical basis for DSI (SLVS) has two distinct modes of operation, each with its own set of electrical  
486 parameters.

487 The PHY layer is described in [MIPI04].

488 **Lane Management Layer:** DSI is Lane-scalable for increased performance. The number of data signals  
489 may be 1, 2, 3, or 4 depending on the bandwidth requirements of the application. The transmitter side of the  
490 interface distributes the outgoing data stream to one or more Lanes (“distributor” function). On the

491 receiving end, the interface collects bytes from the Lanes and merges them together into a recombined data  
492 stream that restores the original stream sequence (“merger” function).

493 **Protocol Layer:** At the lowest level, DSI protocol specifies the sequence and value of bits and bytes  
494 traversing the interface. It specifies how bytes are organized into defined groups called packets. The  
495 protocol defines required headers for each packet, and how header information is generated and interpreted.  
496 The transmitting side of the interface appends header and error-checking information to data being  
497 transmitted. On the receiving side, the header is stripped off and interpreted by corresponding logic in the  
498 receiver. Error-checking information may be used to test the integrity of incoming data. DSI protocol also  
499 documents how packets may be tagged for interleaving multiple command or data streams to separate  
500 destinations using a single DSI.

501 **Application Layer:** This layer describes higher-level encoding and interpretation of data contained in the  
502 data stream. Depending on the display subsystem architecture, it may consist of pixels having a prescribed  
503 format, or of commands that are interpreted by the display controller inside a display module. The DSI  
504 specification describes the mapping of pixel values, commands and command parameters to bytes in the  
505 packet assembly. See [MIPI01].

## 506 **4.2 Command and Video Modes**

507 DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video  
508 Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The mode  
509 definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict  
510 DSI from operating in other applications.

511 Typically, a peripheral is capable of Command Mode operation or Video Mode operation. Some Video  
512 Mode display modules also include a simplified form of Command Mode operation in which the display  
513 module may refresh its screen from a reduced-size, or partial, frame buffer, and the interface (DSI) to the  
514 host processor may be shut down to reduce power consumption.

### 515 **4.2.1 Command Mode**

516 Command Mode refers to operation in which transactions primarily take the form of sending commands  
517 and data to a peripheral, such as a display module, that incorporates a display controller. The display  
518 controller may include local registers and a frame buffer. Systems using Command Mode write to, and read  
519 from, the registers and frame buffer memory. The host processor indirectly controls activity at the  
520 peripheral by sending commands, parameters and data to the display controller. The host processor can also  
521 read display module status information or the contents of the frame memory. Command Mode operation  
522 requires a bidirectional interface.

### 523 **4.2.2 Video Mode Operation**

524 Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of  
525 a real-time pixel stream. In normal operation, the display module relies on the host processor to provide  
526 image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video  
527 information should only be transmitted using High Speed Mode.

528 Some Video Mode architectures may include a simple timing controller and partial frame buffer, used to  
529 maintain a partial-screen or lower-resolution image in standby or Low Power Mode. This permits the  
530 interface to be shut down to reduce power consumption.

531 To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data  
532 path.

**533 4.2.3 Virtual Channel Capability**

534 While this specification only addresses the connection of a host processor to a single peripheral, DSI  
535 incorporates a virtual channel capability for communication between a host processor and multiple,  
536 physical display modules. . A bridge device may create multiple, separate connections to display modules  
537 or other devices or a display module or device may support multiple virtual channels. Display modules are  
538 completely independent, may operate simultaneously, and may be of different display architecture types,  
539 limited only by the total bandwidth available over the shared DSI Link. The details of connecting multiple  
540 peripherals to a single Link are beyond the scope of this document.

541 Since interface bandwidth is shared between peripherals, there are constraints that limit the physical extent  
542 and performance of multiple-peripheral systems.

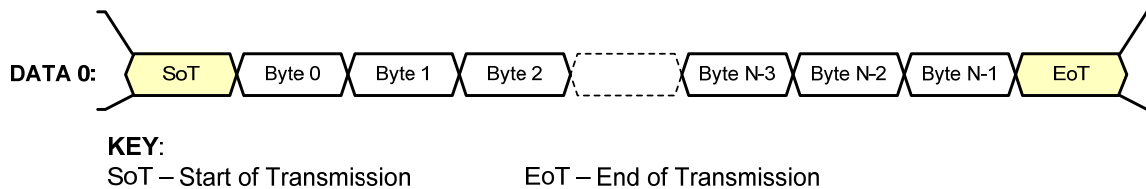
543 The DSI protocol permits up to four virtual channels, enabling traffic for multiple peripherals to share a  
544 common DSI Link. For example, in some high-resolution display designs, multiple physical drivers serve  
545 different areas of a common display panel. Each driver is integrated with its own display controller that  
546 connects to the host processor through DSI. Using virtual channels, the display controller directs data to the  
547 individual drivers, eliminating the need for multiple interfaces or complex multiplexing schemes. Virtual  
548 channels may also be employed by devices where one channel is a bidirectional Command Mode channel  
549 and the second channel is a Video Mode unidirectional channel. Virtual channels may be employed by a  
550 display module or a DSI bridge device receiving interlaced video from the host-processor, where one  
551 channel is corresponding to the first field and another channel is the second field of an interlaced video  
552 frame. The DSI specification makes no requirements on the specific value assigned to each virtual channel  
553 used to designate interlaced fields, For clarity, the first interlaced video field may be assigned as DI[7:6] =  
554 0b00 and the second interlaced video field may be assigned DI[7:6] = 0b01.  
555

## 556 5 DSI Physical Layer

557 This section provides a brief overview of the physical layer used in DSI. See [MIPI04] for more details.

558 Information is transferred between host processor and peripheral using one or more serial data signals and  
 559 accompanying serial clock. The action of sending high-speed serial data across the bus is called a *HS*  
 560 *transmission* or *burst*.

561 Between transmissions, the differential data signal or Lane goes to a low-power state (LPS). Interfaces  
 562 should be in LPS when they are not actively transmitting or receiving high-speed data. Figure 3 shows the  
 563 basic structure of a HS transmission.  $N$  is the total number of bytes sent in the transmission.



566 **Figure 3 Basic HS Transmission Structure**

566 D-PHY low-level protocol specifies a minimum data unit of one byte, and a transmission contains an  
 567 integer number of bytes.

### 568 5.1 Data Flow Control

569 There is no handshake between the Protocol and PHY layers that permit the Protocol layer to throttle data  
 570 transfer to, or from, the PHY layer once transmission is underway. Packets shall be sent and received in  
 571 their entirety and without interruption. The Protocol layer and data buffering on both ends of the Link shall  
 572 always have bandwidth equal to, or greater than, PHY layer circuitry. A practical consequence is that the  
 573 system implementer should ensure that receivers have bandwidth capability that is equal to, or greater than,  
 574 that of the transmitter.

### 575 5.2 Bidirectionality and Low Power Signaling Policy

576 The physical layer for a DSI implementation is composed of one to four Data Lanes and one Clock Lane. In  
 577 a Command Mode system, Data Lane 0 shall be bidirectional; additional Data Lanes shall be unidirectional.  
 578 In a Video Mode system, Data Lane 0 may be bidirectional or unidirectional; additional Data Lanes shall be  
 579 unidirectional. See sections 5.3 and 5.4 for details.

580 For both interface types, the Clock Lane shall be driven by the host processor only, never by the peripheral.

581 Forward direction Low Power transmissions shall use Data Lane 0 only. Reverse direction transmissions on  
 582 Data Lane 0 shall use Low Power Mode only. The peripheral shall be capable of receiving any transmission  
 583 in Low Power or High Speed Mode. Note that transmission bandwidth is substantially reduced when  
 584 transmitting in LP mode.

585 For bidirectional Lanes, data shall be transmitted in the peripheral-to-processor, or reverse, direction using  
 586 Low-Power (LP) Mode only. See [MIPI04] for details on the different modes of transmission.

587 The interface between PHY and Protocol layers has several signals controlling bus direction. When a host  
 588 transmitter requires a response from a peripheral, e.g. returning READ data or status information, it asserts  
 589 TurnRequest to its PHY during the last packet of the transmission. This tells the PHY layer to assert the  
 590 Bus Turn-Around (BTA) command following the EoT sequence.

591 When a peripheral receives the Bus Turn-Around command, its PHY layer asserts TurnRequest as an input  
 592 to the Protocol layer. This tells the receiving Protocol layer that it shall prepare to send a response to the  
 593 host processor. Normally, the packet just received tells the Protocol layer what information to send once the  
 594 bus is available for transmitting to the host processor.

595 After transmitting its response, the peripheral similarly hands bus control back to the host processor using a  
 596 TurnRequest to its own PHY layer.

### 597 **5.3 Command Mode Interfaces**

598 The minimum physical layer requirement for a DSI host processor operating in Command Mode is:

- 599 • Data Lane Module: CIL-MFAA (HS-TX, LP-TX, LP-RX, and LP-CD)
- 600 • Clock Lane Module: CIL-MCNN (HS-TX, LP-TX)

601 The minimum physical layer requirement for a DSI peripheral operating in Command Mode is:

- 602 • Data Lane Module: CIL-SFAA (HS-RX, LP-RX, LP-TX, and LP-CD)
- 603 • Clock Lane Module: CIL-SCNN (HS-RX, LP-RX)

604 A Bidirectional Link shall support reverse-direction Escape Mode for Data Lane 0 to support LPDT for  
 605 read data as well as ACK and TE Trigger Messages issued by the peripheral. In the forward direction, Data  
 606 Lane 0 shall support LPDT as described in [MIPI04]. All Trigger messages shall be communicated across  
 607 Data Lane 0.

### 608 **5.4 Video Mode Interfaces**

609 The minimum physical layer requirement for a DSI transmitter operating in Video Mode is:

- 610 • Data Lane Module: CIL-MFAN (HS-TX, LP-TX)
- 611 • Clock Lane Module: CIL-MCNN (HS-TX, LP-TX)

612 The minimum physical layer requirement for a DSI receiver operating in Video Mode is:

- 613 • Data Lane Module: CIL-SFAN (HS-RX, LP-RX)
- 614 • Clock Lane Module: CIL-SCNN (HS-RX, LP-RX)

615 In the forward direction, Data Lane 0 shall support LPDT as described in [MIPI04]. All Trigger messages  
 616 shall be communicated across Data Lane 0.

### 617 **5.5 Bidirectional Control Mechanism**

618 Turning the bus around is controlled by a token-passing mechanism: the host processor sends a Bus Turn-  
 619 Around (BTA) request, which conveys to the peripheral its intention to release, or stop driving, the data  
 620 path after which the peripheral can transmit one or more packets back to the host processor. When it is  
 621 finished, the peripheral shall return control of the bus back to the host processor. Bus Turn-Around is  
 622 signaled using an Escape Mode mechanism provided by PHY-level protocol.

623 In bidirectional systems, there is a remote chance of erroneous behavior due to EMI that could result in bus  
624 contention. Mechanisms are provided in this specification for recovering from any bus contention event  
625 without forcing “hard reset” of the entire system.

## 626 5.6 Clock Management

627 DSI Clock is a signal from the host processor to the peripheral. In some systems, it may serve multiple  
628 functions:

629 **DSI Bit Clock:** Across the Link, DSI Clock is used as the source-synchronous bit clock for capturing serial  
630 data bits in the receiver PHY. This clock shall be active while data is being transferred.

631 **Byte Clock:** Divided down, DSI Clock is used to generate a byte clock at the conceptual interface between  
632 the Protocol and Application layers. During HS transmission, each byte of data is accompanied by a byte  
633 clock. Like the DSI Bit Clock, the byte clock shall be active while data is being transferred. At the Protocol  
634 layer to Application layer interface, all actions are synchronized to the byte clock.

635 **Application Clock(s):** Divided-down versions of DSI Bit Clock may be used for other clocked functions at  
636 the peripheral. These “application clocks” may need to run at times when no serial data is being transferred,  
637 or they may need to run constantly (continuous clock) to support active circuitry at the peripheral. Details  
638 of how such additional clocks are generated and used are beyond the scope of this document.

639 For continuous clock behavior, the Clock Lane remains in high-speed mode generating active clock signals  
640 between HS data packet transmissions. For non-continuous clock behavior, the Clock Lane enters the LP-  
641 11 state between HS data packet transmissions.

### 642 5.6.1 Clock Requirements

643 All DSI transmitters and receivers shall support continuous clock behavior on the Clock Lane, and  
644 optionally may support non-continuous clock behavior. A DSI host processor shall support continuous  
645 clock for systems that require it, as well as having the capability of shutting down the serial clock to reduce  
646 power.

647 Note that the host processor controls the desired mode of clock operation. Host protocol and applications  
648 control Clock Lane operating mode (High Speed or Low Power mode). System designers are responsible  
649 for understanding the clock requirements for peripherals attached to DSI and controlling clock behavior in  
650 accordance with those requirements.

651 Note that in Low Power signaling mode, LP clock is functionally embedded in the data signals. When LP  
652 data transmission ends, the clock effectively stops and subsequent LP clocks are not available to the  
653 peripheral. The peripheral shall not require additional bits, bytes, or packets from the host processor in  
654 order to complete processing or pipeline movement of received data in LP mode transmissions. There are a  
655 variety of ways to meet this requirement. For example, the peripheral may generate its own clock or it may  
656 require the host processor to keep the HS serial clock running.

657 The handshake process for BTA allows only limited mismatch of Escape Mode clock frequencies between  
658 a host processor and a peripheral. The Escape Mode frequency ratio between host processor and peripheral  
659 shall not exceed 3:2. The host processor is responsible for controlling its own clock frequency to match the  
660 peripheral. The host processor LP clock frequency shall be in the range of 67% to 150% of peripheral LP  
661 clock frequency. Therefore, the peripheral implementer shall specify a peripheral’s nominal LP clock  
662 frequency and the guaranteed accuracy.

## 663 5.6.2 Clock Power and Timing

664 Additional timing requirements in [MIPI04] specify the timing relationship between the power state of data  
665 signal(s) and the power state of the clock signal. It is the responsibility of the host processor to observe this  
666 timing relationship. If the DSI Clock runs continuously, these timing requirements do not apply.

## 667 5.7 System Power-Up and Initialization

668 System power-up is a multi-state process that depends not only on initialization of the master (host  
669 processor) and slave (peripheral) devices, but also possibly on internal delays within the slave device. This  
670 section specifies the parameters necessary for operation, and makes several recommendations to help  
671 ensure the system power-up process is robust.

672 After power-up, the host processor shall observe an initialization period,  $T_{INIT}$ , during which it shall drive a  
673 sustained TX-Stop state (LP-11) on all Lanes of the Link. See [MIPI04] for descriptions of  $T_{INIT}$  and the  
674 TX-Stop state.

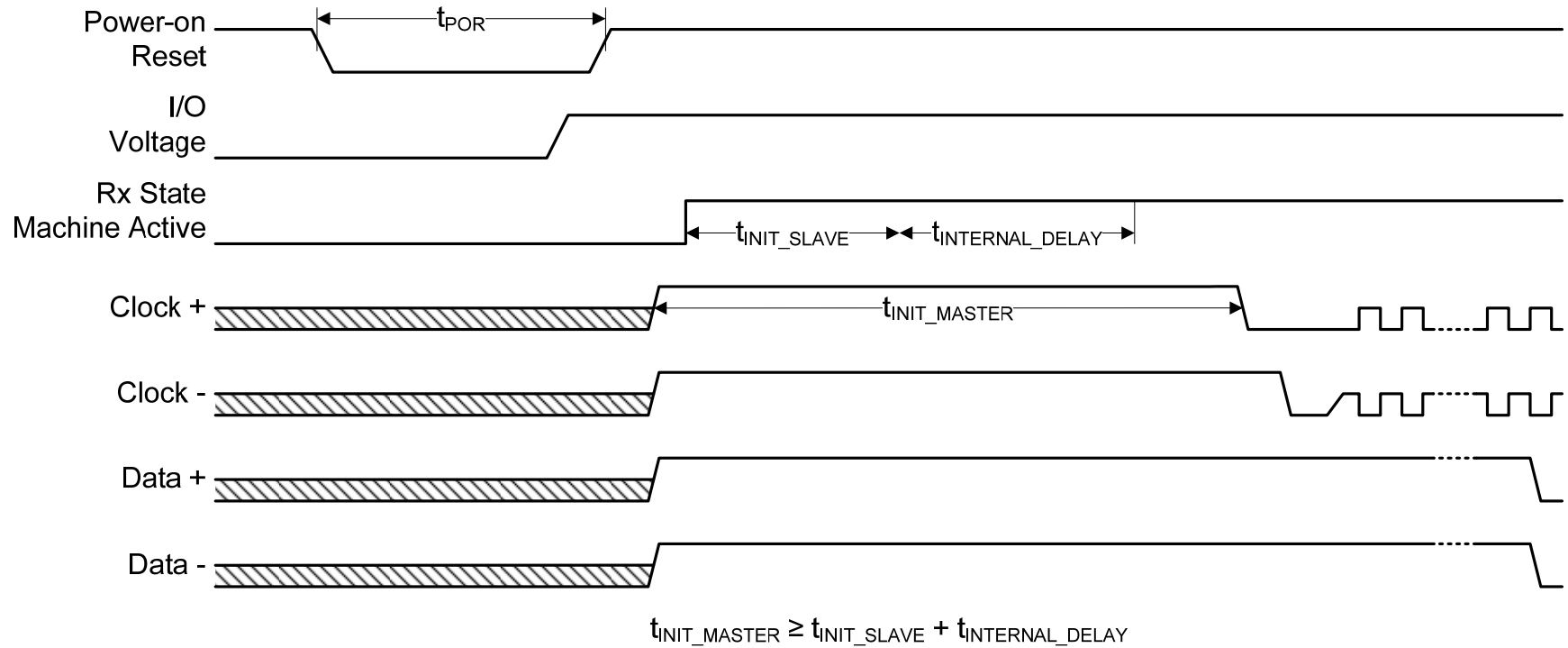
675 Peripherals shall power up in the RX-Stop state and monitor the Link to determine if the host processor has  
676 asserted a TX-Stop state for at least the  $T_{INIT}$  period. The peripheral shall ignore all Link states prior to  
677 detection of a  $T_{INIT}$  event. The peripheral shall be ready to accept bus transactions immediately following  
678 the end of the  $T_{INIT}$  period.

679 Detecting the  $T_{INIT}$  event requires some minimal timing capability on the peripheral. However, accuracy is  
680 not critical as long as a  $T_{INIT}$  event can be reliably detected; an R-C timer with  $\pm 30\%$  accuracy is acceptable  
681 in most cases.

682 If the peripheral requires a longer period after power-up than the  $T_{INIT}$  period driven by the host processor,  
683 this requirement shall be declared in peripheral product information or data sheets. The host processor shall  
684 observe the required additional time after peripheral power-up.


685 Figure 4 illustrates an example power-up sequence for a DSI display module. In the figure, a power-on  
686 reset (POR) mechanism is assumed for initialization. Internally within the display module, de-assertion of  
687 POR could happen after both I/O and core voltages are stable. The worst case  $t_{POR}$  parameter can be defined  
688 by the display module data sheet.  $t_{INIT\_SLAVE}$  represents the minimum initialization period ( $T_{INIT}$ ) defined in  
689 [MIPI04] for a host driving LP-11 to the display. This interval starts immediately after the  $t_{POR}$  period. The  
690 peripheral might need an additional  $t_{INTERNAL\_DELAY}$  time to reach a functional state after power-up. In this  
691 case,  $t_{INTERNAL\_DELAY}$  should also be defined in the display module data sheet. In this example, the host's  
692  $t_{INIT\_MASTER}$  parameter is programmed for driving LP-11 for a period longer than the sum of  $t_{INIT\_SLAVE}$  and  
693  $t_{INTERNAL\_DELAY}$ . The display module ignores all Lane activities during this time.





694

695

 Any drive state except LP-11, LP-10 or LP-01

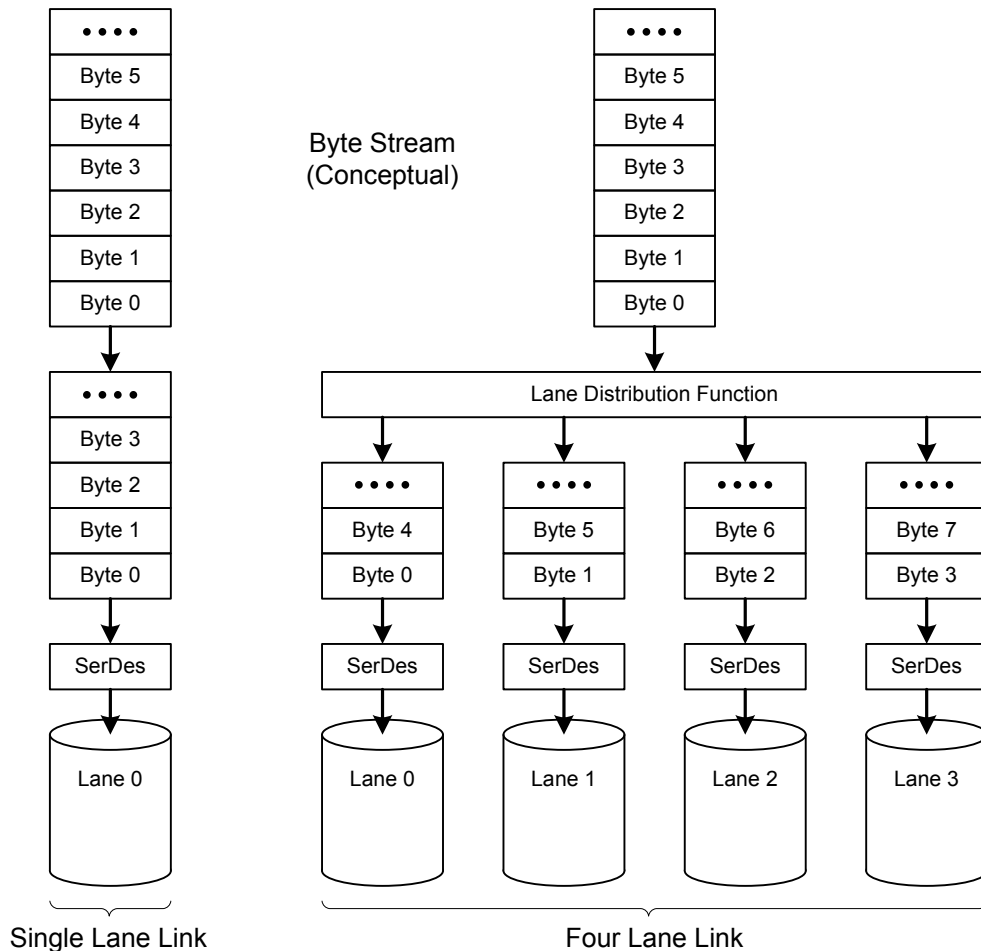
**Figure 4 Peripheral Power-Up Sequencing Example**

696 **6 Multi-Lane Distribution and Merging**

697 DSI is a Lane-scalable interface. Applications requiring more bandwidth than that provided by one Data  
 698 Lane may expand the data path to two, three, or four Lanes wide and obtain approximately linear increases  
 699 in peak bus bandwidth. This document explicitly defines the mapping between application data and the  
 700 serial bit stream to ensure compatibility between host processors and peripherals that make use of multiple  
 701 Lanes.

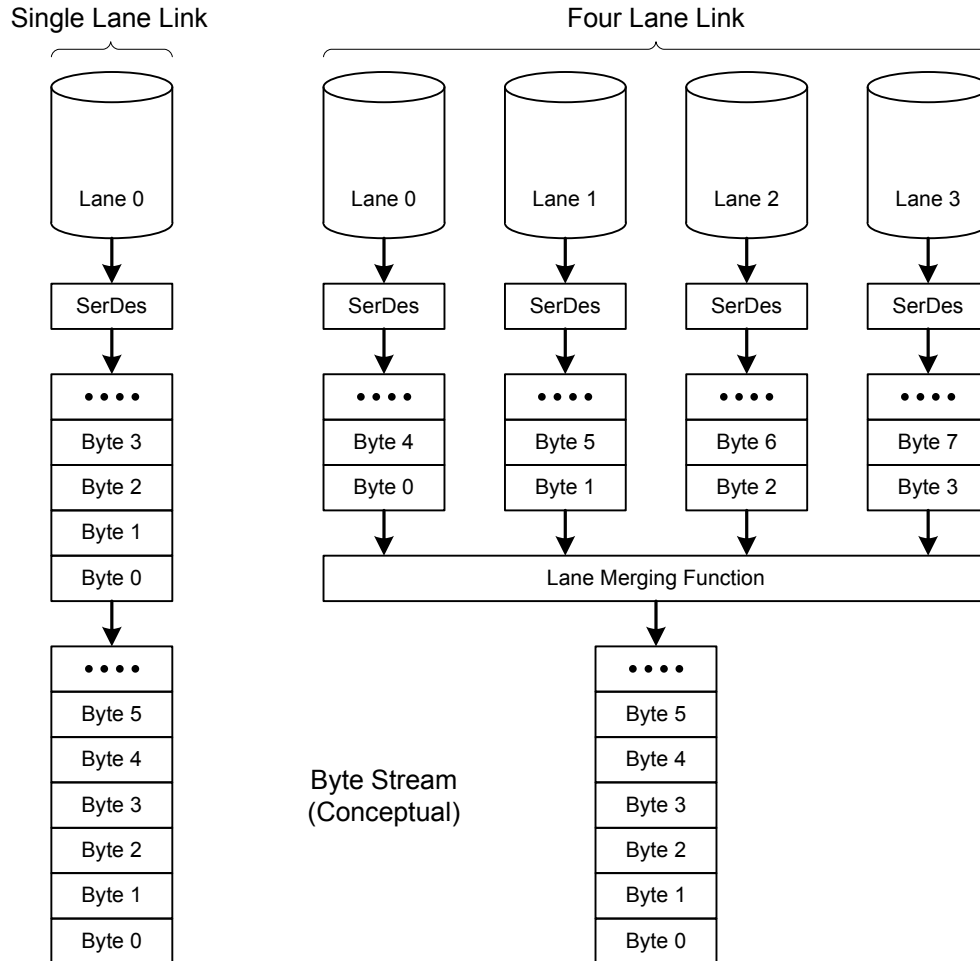
702 Multi-Lane implementations shall use a single common clock signal, shared by all Data Lanes.

703 Conceptually, between the PHY and higher functional blocks is a layer that enables multi-Lane operation.  
 704 In the transmitter, shown in Figure 5, this layer distributes a sequence of packet bytes across N Lanes,  
 705 where each Lane is an independent block of logic and interface circuitry. In the receiver, shown in Figure 6,  
 706 the layer collects incoming bytes from N Lanes and consolidates the bytes into complete packets to pass  
 707 into the following packet decomposer.



708  
 709

**Figure 5 Lane Distributor Conceptual Overview**



710

711

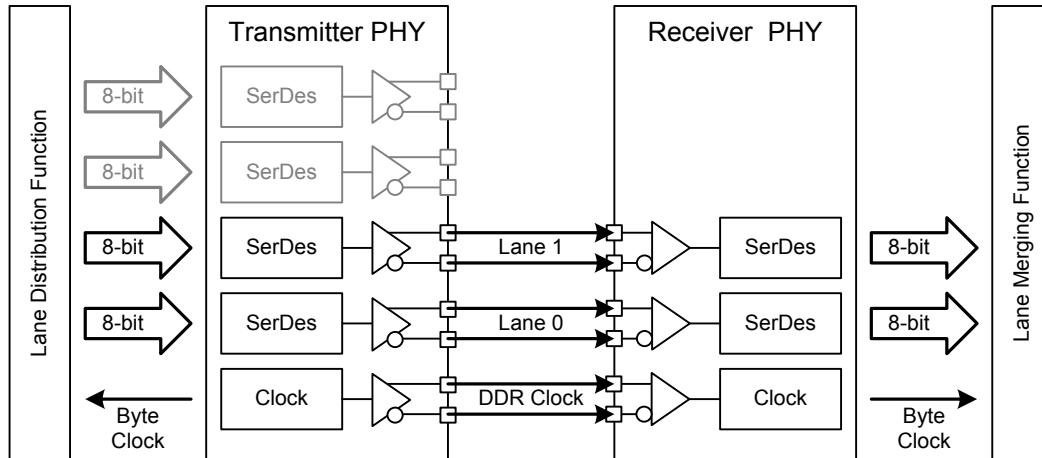
**Figure 6 Lane Merger Conceptual Overview**

712 The Lane Distributor takes a HS transmission of arbitrary byte length, buffers N bytes, where N is the  
 713 number of Lanes implemented in the interface, and sends groups of N bytes in parallel across the N Lanes.  
 714 Before sending data, all Lanes perform the SoT sequence in parallel to indicate to their corresponding  
 715 receiving units that the first byte of a packet is beginning. After SoT, the Lanes send groups of N bytes  
 716 from the first packet in parallel, following a round-robin process. For example, with a two Lane system,  
 717 byte 0 of the packet goes to Lane 0, byte 1 goes to Lane 1, byte 2 to Lane 0, byte 3 to Lane 1 and so on.

## 718 6.1 Multi-Lane Interoperability and Lane-number Mismatch

719 The number of Lanes used shall be a static parameter. It shall be fixed at the time of system design or initial  
 720 configuration and may not change dynamically. Typically, the peripheral's bandwidth requirement and its  
 721 corresponding Lane configuration establishes the number of Lanes used in a system.

722 The host processor shall be configured to support the same number of Lanes required by the peripheral.  
 723 Specifically, a host processor with N-Lane capability ( $N > 1$ ) shall be capable of operation using fewer  
 724 Lanes, to ensure interoperability with peripherals having M Lanes, where  $N > M$ .



725

726

**Figure 7 Four-Lane Transmitter with Two-Lane Receiver Example**

727

### 6.1.1 Clock Considerations with Multi-Lane

728 At EoT, the Protocol layer shall base its control of the common DSI Clock signal on the timing  
 729 requirements for the last active Lane Module. If the Protocol layer puts the DSI Clock into LPS between  
 730 HS transmissions to save power, it shall respect the timing requirement for DSI Clock relative to all serial  
 731 data signals during the EoT sequence.

732 Prior to SoT, timing requirements for DSI Clock startup relative to all serial data signals shall similarly be  
 733 respected.

734

### 6.1.2 Bidirectionality and Multi-Lane Capability

735 Peripherals typically do not have substantial bandwidth requirements for returning data to the host  
 736 processor. To keep designs simple and improve interoperability, all DSI-compliant systems shall only use  
 737 Lane 0 in LP Mode for returning data from a peripheral to the host processor.

738

### 6.1.3 SoT and EoT in Multi-Lane Configurations

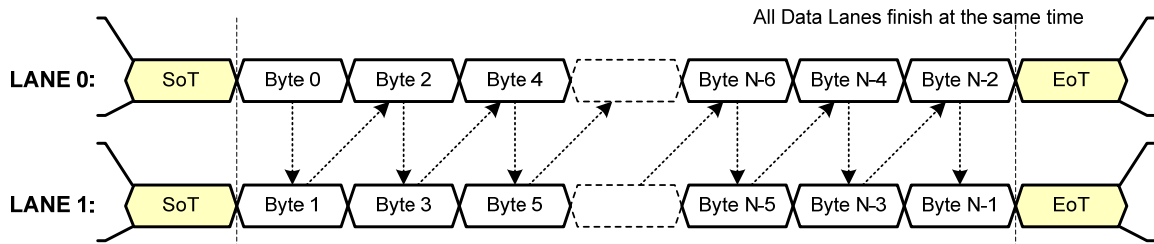
739 Since a HS transmission is composed of an arbitrary number of bytes that may not be an integer multiple of  
 740 the number of Lanes, some Lanes may run out of data before others. Therefore, the Lane Management  
 741 layer, as it buffers up the final set of less-than-N bytes, de-asserts its “valid data” signal into all Lanes for  
 742 which there is no further data.

743 Although all Lanes start simultaneously with parallel SoTs, each Lane operates independently and may  
 744 complete the HS transmission before the other Lanes, sending an EoT one cycle (byte) earlier.

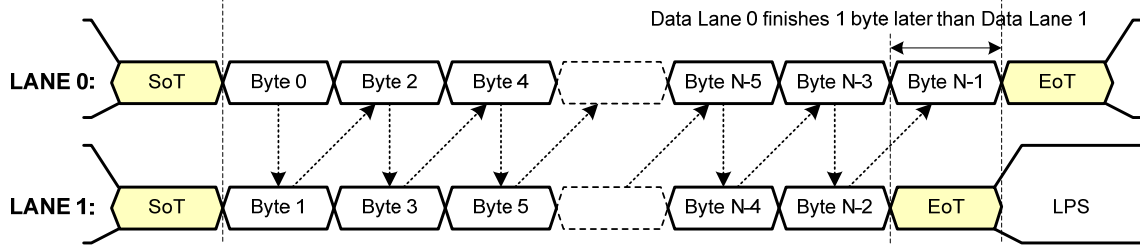
745 The N PHYs on the receiving end of the Link collect bytes in parallel and feed them into the Lane  
 746 Management layer. The Lane Management layer reconstructs the original sequence of bytes in the  
 747 transmission.

748 Figure 8 and Figure 9 illustrate a variety of ways a HS transmission can terminate for different number of  
 749 Lanes and packet lengths.

Number of Bytes, N, transmitted is an integer multiple of the number of lanes:



Number of Bytes, N, transmitted is NOT an integer multiple of the number of lanes:



**KEY:**

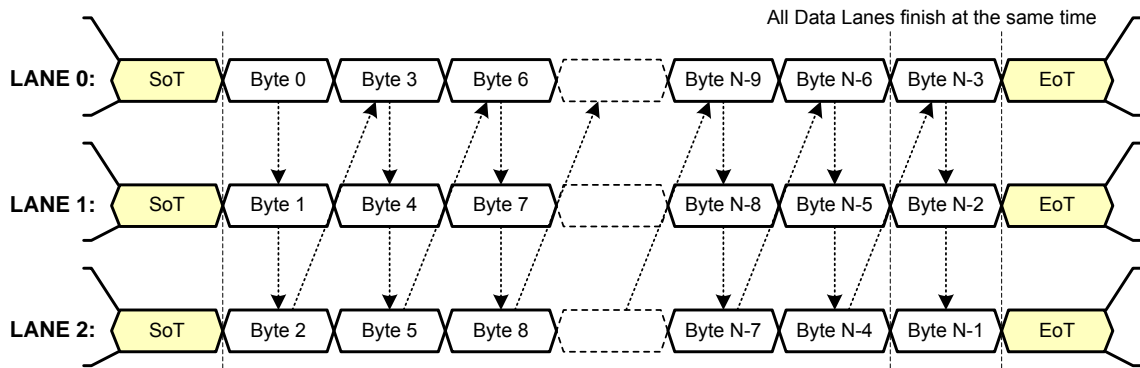
LPS – Low Power State      SoT – Start of Transmission      EoT – End of Transmission

750

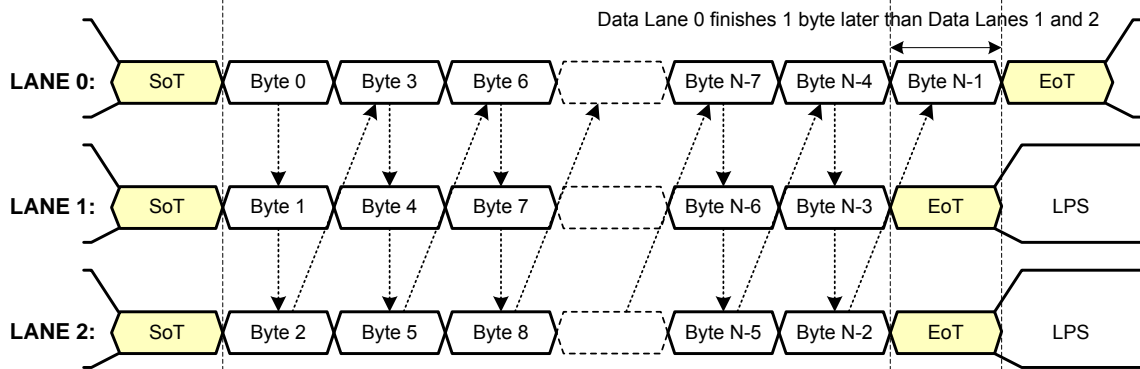
751

**Figure 8 Two Lane HS Transmission Example**

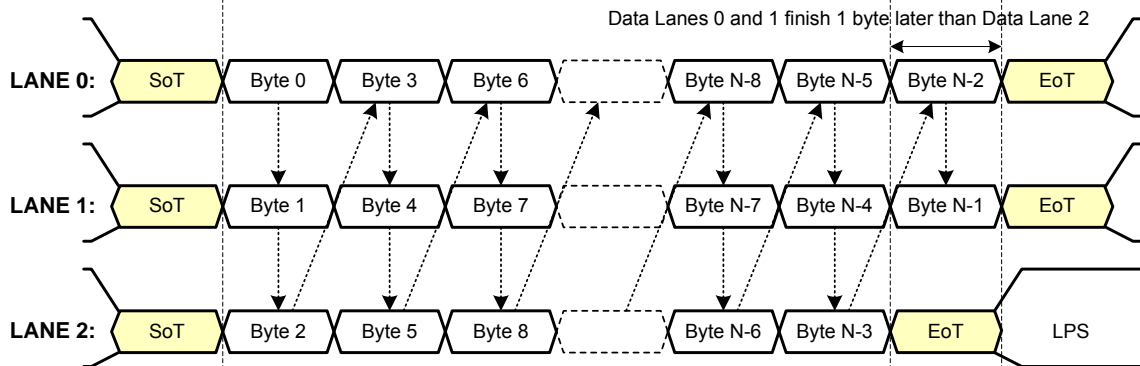
Number of Bytes, N, transmitted is an integer multiple of the number of lanes:



Number of Bytes, N, transmitted is NOT an integer multiple of the number of lanes (Example 1):



Number of Bytes, N, transmitted is NOT an integer multiple of the number of lanes (Example 2):



KEY:

LPS – Low Power State      SoT – Start of Transmission      EoT – End of Transmission

Figure 9 Three Lane HS Transmission Example

752

753

754

## 755 **7 Low-Level Protocol Errors and Contention**

756 For DSI systems there is a possibility that EMI, ESD or other transient-error mechanisms might cause one  
757 end of the Link to go to an erroneous state, or for the Link to transmit corrupted data.

758 In some cases, a transient error in a state machine, or in a clock or data signal, may result in detectable low-  
759 level protocol errors that indicate associated data is, or is likely to be, corrupt. Mechanisms for detecting  
760 and responding to such errors are detailed in the following sections.

761 In other cases, a bidirectional PHY that should be receiving data could begin transmitting while the  
762 authorized transmitter is simultaneously driving the same data line, causing contention and lost data.

763 This section documents the minimum required functionality for recovering from certain low-level protocol  
764 errors and contention. Low-level protocol errors are detected by logic in the PHY, while contention  
765 problems are resolved using contention detectors and timers. Actual contention in DSI-based systems will  
766 be very rare. In most cases, the appropriate use of timers enables recovery from a transient contention  
767 situation.

768 Note that contention-related features are of no benefit for unidirectional DSI Links. However, the “common  
769 mode fault” can still occur in unidirectional systems.

770 The following sections specify the minimum required functionality for detection of low-level protocol  
771 errors, for contention recovery, and associated timers for host processors and peripherals using DSI.

### 772 **7.1 Low-Level Protocol Errors**

773 Logic in the PHY can detect some classes of low-level protocol errors. These errors shall be communicated  
774 to the Protocol layer via the PHY-Protocol Interface. The following errors shall be identified and stored by  
775 the peripheral as status bits for later reporting to the host processor:

- 776 • SoT Error
- 777 • SoT Sync Error
- 778 • EoT Sync Error
- 779 • Escape Mode Entry Command Error
- 780 • LP Transmission Sync Error
- 781 • False Control Error

782 The mechanism for reporting and clearing these error bits is detailed in section 8.10.7. Note that  
783 unidirectional DSI peripherals are exempt from the reporting requirement since they cannot report such  
784 errors to the host processor.

#### 785 **7.1.1 SoT Error**

786 The leader sequence for Start of High-Speed Transmission (SoT) is fault tolerant for any single-bit error  
787 and some multi-bit errors. The received synchronization bits and following data packet might therefore still  
788 be uncorrupted if an error is detected, but confidence in the integrity of payload data is lower. This  
789 condition shall be communicated to the protocol with *SoT Error* flag.

790

**Table 1 Sequence of Events to Resolve SoT Error (HS RX Side)**

PHY	Protocol
Detect SoT Error	
Assert <i>SoT Error</i> flag to protocol	Receive and store <i>SoT Error</i> flag
	Send <i>SoT Error</i> in <i>Acknowledge and Error Report</i> packet, if requested; take no other action based on received HS transmission

791 *SoT Error* is detected by the peripheral PHY. If an acknowledge response is expected, the peripheral shall  
 792 send a response using Data Type 0x02 (*Acknowledge and Error Report*) and set the *SoT Error* bit in the  
 793 return packet to the host processor. The peripheral should take no other action based on the potentially  
 794 corrupted received HS transmission.

### 795 7.1.2 SoT Sync Error

796 If the SoT leader sequence is corrupted in a way that proper synchronization cannot be expected, *SoT Sync*  
 797 *Error* shall be flagged. Subsequent data in the HS transmission is probably corrupt and should not be used.

798

**Table 2 Sequence of Events to Resolve SoT Sync Error (HS RX Side)**

PHY	Protocol
Detect <i>SoT Sync Error</i>	
Assert <i>SoT Sync Error</i> to protocol	Receive and store <i>SoT Sync Error</i> flag
May choose not to pass corrupted data to Protocol layer	Send <i>SoT Sync Error</i> with <i>Acknowledge and Error Report</i> packet if requested; take no other action based on received transmission

799 *SoT Sync Error* is detected by the peripheral PHY. If an acknowledge response is expected, the peripheral  
 800 shall send a response using Data Type 0x02 (*Acknowledge and Error Report*) and set the *SoT Sync Error*  
 801 bit in the return packet to the host processor. Since data is probably corrupted, no command shall be  
 802 interpreted or acted upon in the peripheral. No WRITE activity shall be undertaken in the peripheral.

### 803 7.1.3 EoT Sync Error

804 DSI is a byte-oriented protocol. All uncorrupted HS transmissions contain an integer number of bytes. If,  
 805 during EoT sequence, the peripheral PHY detects that the last byte does not match a byte boundary, *EoT*  
 806 *Sync Error* shall be flagged. If an *Acknowledge* response is expected, the peripheral shall send an  
 807 *Acknowledge and Error Report* packet. The peripheral shall set the *EoT Sync Error* bit in the Error Report  
 808 bytes of the return packet to the host processor.

809 If possible, the peripheral should take no action, especially WRITE activity, in response to the intended  
 810 command. Since this error is not recognized until the end of the packet, some irreversible actions may take  
 811 place before the error is detected.



812

**Table 3 Sequence of Events to Resolve EoT Sync Error (HS RX Side)**

Receiving PHY	Receiving Protocol
Detect EoT Sync Error	
Notify Protocol of <i>EoT Sync Error</i>	Receive and store <i>EoT Sync Error</i> flag
	Ignore HS transmission if possible; assert <i>EoT Sync Error</i> if Acknowledge is requested

813

**7.1.4 Escape Mode Entry Command Error**

814 If the Link begins an Escape Mode sequence, but the Escape Mode Entry command is not recognized by  
 815 the receiving PHY Lane, the receiver shall flag *Escape Mode Entry Command* error. This scenario could be  
 816 a legitimate command, from the transmitter point of view, that's not recognized or understood by the  
 817 receiving protocol. In bidirectional systems, receivers in both ends of the Link shall detect and flag  
 818 unrecognized Escape Mode sequences. Only the peripheral reports this error.

819

**Table 4 Sequence of Events to Resolve Escape Mode Entry Command Error (RX Side)**

Receiving PHY	Receiving Protocol
Detect <i>Escape Mode Entry Command</i> Error	
Notify Protocol of <i>Escape Mode Entry Command</i> Error	Observe <i>Escape Mode Entry Command</i> Error flag
Go to <i>Escape Wait</i> until Stop state is observed	Ignore Escape Mode transmission (if any)
Observe <i>Stop</i> state	
Return to LP-RX Control mode	set Escape Mode Entry Command Error bit

820

**7.1.5 LP Transmission Sync Error**

821 This error flag is asserted if received data is not synchronized to a byte boundary at the end of Low-Power  
 822 Transmission. In bidirectional systems, receivers in both ends of the Link shall detect and flag LP  
 823 Transmission Sync errors. Only the peripheral reports this error.

824

**Table 5 Sequence of Events to Resolve LP Transmission Sync Error (RX Side)**

Receiving PHY	Receiving Protocol
Detect <i>LP Transmission Sync Error</i>	
Notify Protocol of <i>LP Transmission Sync Error</i>	Receive <i>LP Transmission Sync Error</i> flag
Return to <i>LP-RX Control</i> mode until Stop state is observed	Ignore Escape Mode transmission if possible, set appropriate error bit and wait

825

**7.1.6 False Control Error**

826 If a peripheral detects LP-10 (LP request) not followed by the remainder of a valid escape or turnaround  
 827 sequence or if it detects LP-01 (HS request) not followed by a bridge state (LP-00), a False Control Error  
 828 shall be captured in the error status register and reported back to the host after the next BTA. This error  
 829 should be flagged locally to the receiving protocol layer, e.g. when a host detects LP-10 not followed by the  
 830 remainder of a valid escape or turnaround sequence.

831

**Table 6 Sequence of Events to Resolve False Control Error (RX Side)**

Receiving PHY	Receiving Protocol
Detect <i>False Control Error</i>	
Notify Protocol of <i>False Control Error</i>	Observe <i>False Control Error</i> flag, set appropriate error bit and wait
Ignore Turnaround or Escape Mode request	
Remain in <i>LP-RECEIVE STATE Control</i> mode until <i>Stop</i> state is observed	

832

833

**Table 7 Low-Level Protocol Error Detection and Reporting**

Error Detected	HS Unidirectional, LP Unidirectional, no Escape Mode		HS Unidirectional, LP Bidirectional with Escape Mode	
	Host Processor	Peripheral	Host Processor	Peripheral
SoT Error	NA	Detect, no report	NA	Detect and report
SoT Sync Error	NA	Detect, no report	NA	Detect and report
EoT Sync Error	NA	Detect, no report	NA	Detect and report
Escape Mode Entry Command Error	No	No	Detect and flag	Detect and report
LP Transmission Sync Error	No	No	Detect and flag	Detect and report
False Control Error	No	No	Detect and flag	Detect and report

## 834 7.2 Contention Detection and Recovery

835 Contention is a potentially serious problem that, although very rare, could cause the system to hang and  
 836 force a hard reset or power off / on cycle to recover. DSI specifies two mechanisms to minimize this  
 837 problem and enable easier recovery: contention detectors in the PHY for LP Mode contention, and timers  
 838 for other forms of contention and common-mode faults.

### 839 7.2.1 Contention Detection in LP Mode

840 In bidirectional Links, contention detectors in the PHY shall detect two types of contention faults: LP High  
 841 Fault and LP Low Fault. Refer to [MIPI04] for definitions of LP High and LP Low faults. The peripheral  
 842 shall set *Contention Detected* in the Error Report bytes, when it detects either of the contention faults.

843 Annex A provides detailed descriptions and state diagrams for PHY-based detection and recovery  
 844 procedures for LP contention faults. The state diagrams show a sequence of events beginning with  
 845 detection, and ending with return to normal operation.

### 846 7.2.2 Contention Recovery Using Timers

847 The PHY cannot detect all forms of contention. Although they do not directly detect contention, the use of  
 848 appropriate timers ensures that any contention that does happen is of limited duration. The peripheral shall  
 849 set *Peripheral Timeout Error* in the Error Report bytes, when the peripheral detects either HS RX Timer or  
 850 LP TX Timer – Peripheral, defined in section 7.2.2.1, has expired,

851 The time-out mechanisms described in this section are useful for recovering from contention failures,  
852 without forcing the system to undergo a hard reset (power off-on cycle).

### 853 7.2.2.1 Summary of Required Contention Recovery Timers

854 Table 8 specifies the minimum required set of timers for contention recovery in a DSI system.

855 **Table 8 Required Timers and Timeout Summary**

Timer	Timeout	Abbreviation	Requirement
HS RX Timer	HS RX Timeout	HRX_TO	R in bidirectional peripheral
HS TX Timer	HS TX Timeout	HTX_TO	R in host
LP TX Timer – Peripheral	LP_TX-P Timeout	LTX-P_TO	R in bidirectional peripheral
LP RX Timer – Host Processor	LP_RX-H Timeout	LRX-H_TO	R in host

### 856 7.2.2.2 HS RX Timeout (HRX\_TO) in Peripheral

857 This timer is useful for recovering from some transient errors that may result in contention or common-  
858 mode fault. The HRX\_TO timer directly monitors the time a peripheral's HS receiver stays in High-Speed  
859 mode. It is programmed to be longer than the maximum duration of a High-Speed transmission expected by  
860 the peripheral receiver. HS RX timeout will signal an error during HS RX mode if EoT is not received  
861 before the timeout expires.

862 Combined with HTX\_TO, these timers ensure that a transient error will limit contention in HS mode to the  
863 timeout period, and the bus will return to a normal LP state. The Timeout value is protocol specific. HS RX  
864 Timeout shall be used for Bidirectional Links and for Unidirectional Links with Escape Mode. HS RX  
865 Timeout is recommended for all DSI peripherals and required for all bidirectional DSI peripherals.

866 **Table 9 Sequence of Events for HS RX Timeout (Peripheral initially HS RX)**

Host Processor Side	Peripheral Side
Drives bus HS-TX	HS RX Timeout Timer Expires
	Transition to LP-RX
End HS transmission normally, or HS-TX timeout	Peripheral waits for <i>Stop</i> state before responding to bus activity.
Transition to <i>Stop</i> state (LP-11)	Observe <i>Stop</i> state and flag error

867 During this mode, the HS clock is active and can be used for the HS RX Timer in the peripheral.

868 The LP High Fault and LP Low Fault are caused by both sides of the Link transmitting simultaneously.  
869 Note, the LP High Fault and LP Low Fault are only applicable for bidirectional Data Lanes.

870 The Common Mode fault occurs when the transmitter and receiver are not in the same communication  
871 mode, e.g. transmitter (host processor) is driving LP-01 or LP-10, while the receiver (peripheral) is in HS-  
872 RX mode with terminator connected. There is no contention, but the receiver will not capture transmitted  
873 data correctly. This fault may occur in both bidirectional and unidirectional lanes. After HS RX timeout,  
874 the peripheral returns to LP-RX mode and normal operation may resume. Note that in the case of a  
875 common-mode fault, there may be no DSI serial clock from the host processor. Therefore, another clock  
876 source for HRX\_TO timer may be required.

877 **7.2.2.3 HS TX Timeout (HTX\_TO) in Host Processor**

878 This timer is used to monitor a host processor's own length of HS transmission. It is programmed to be  
 879 longer than the expected maximum duration of a High-Speed transmission. The maximum HS transmission  
 880 length is protocol-specific. If the timer expires, the processor forces a clean termination of HS transmission  
 881 and enters EoT sequence, then drives LP-11 state. This timeout is required for all host processors.

882 **Table 10 Sequence of Events for HS TX Timeout (Host Processor initially HS TX)**

Host Processor Side	Peripheral Side
Host Processor in HS TX mode	Peripheral in HS RX mode
HS TX Timeout Timer expires, forces EoT	
Host Processor drives <i>Stop</i> state (LP-11)	Peripheral observes EoT and <i>Stop</i> state (LP-RX)

883 Note that the peripheral HS-RX timeout (see section 7.2.2.2) should be set to a value shorter than the host  
 884 processor's HS-TX timer so that the peripheral has returned to LP-RX state and is ready for further  
 885 commands following receipt of LP-11 from the host processor.

886 **7.2.2.4 LP TX-Peripheral Timeout (LTX-P\_TO)**

887 This timer is used to monitor the peripheral's own length of LP transmission (bus possession time) when in  
 888 LP TX mode. The maximum transmission length in LP TX is determined by protocol and data formats.  
 889 This timeout is useful for recovering from LP-contention. LP TX-Peripheral Timeout is required for  
 890 bidirectional peripherals.

891 **Table 11 Sequence of Events for LP TX-Peripheral Timeout (Peripheral initially LP TX)**

Host Processor Side	Peripheral Side
(possible contention)	Peripheral in LP TX mode
	LP TX-P Timeout Timer Expires
	Transition to LP-RX
Detect contention, or Host LP-RX Timeout	Peripheral waits for <i>Stop</i> state before responding to bus activity.
Drive LP-11 <i>Stop</i> state	Observe <i>Stop</i> state in LP-RX mode

892 Note that host processor LP-RX timeout (see section 7.2.2.5) should be set to a *longer* value than the  
 893 peripheral's LP-TX-P timer, so that the peripheral has returned to LP-RX state and is ready for further  
 894 commands following receipt of LP-11 from the host processor.

895 **7.2.2.5 LP-RX Host Processor Timeout (LRX-H\_TO)**

896 The LP-RX timeout period in the Host Processor shall be greater than the LP TX-Peripheral timeout. Since  
 897 both timers begin counting at approximately the same time, this ensures the peripheral has returned to LP-  
 898 RX mode and is waiting for bus activity (commands from Host Processor, etc.) when LP-RX timer expires  
 899 in the host. The timeout value is protocol specific. This timer is required for all Host Processors.

900 **Table 12 Sequence of Events for Host Processor Wait Timeout (Peripheral initially TX)**

Host Processor Side	Peripheral Side
Host Processor in LP RX mode	(peripheral LP-TX timeout)

Host Processor Side	Peripheral Side
Host Processor LP-RX Timer expires	Peripheral waiting in LP-RX mode
Host Processor drives <i>Stop</i> state (LP-11)	Peripheral observes <i>Stop</i> state in LP-RX mode

901 **7.3 Additional Timers**

902 Additional timers are used to detect bus turnaround problems and to ensure sufficient wait time after a  
903 RESET Trigger Message is sent to the peripheral.

904 **7.3.1 Turnaround Acknowledge Timeout (TA\_TO)**

905 When either end of the Link issues BTA (Bus Turn-Around), its PHY shall monitor the sequence of Data  
906 Lane states during the ensuing turnaround process. In a normal BTA sequence, the turnaround completes  
907 within a bounded time, with the other end of the Link finally taking bus possession and driving LP-11 (*Stop*  
908 *state*) on the bus. If the sequence is observed not to complete (by the previously-transmitting PHY) within  
909 the specified time period, the timer TA\_TO expires. The side of the Link that issued the BTA then begins a  
910 recovery procedure, or re-sends BTA. The specified period shall be longer than the maximum possible  
911 turnaround delay for the unit to which the turnaround request was sent. TA\_TO is an optional timer.

912 **Table 13 Sequence of Events for BTA Acknowledge Timeout (Peripheral initially TX)**

Host Processor Side	Peripheral Side
Host in LP RX mode	Peripheral in LP TX mode
	Send Turnaround back to Host
(no change)	Turnaround Acknowledgement Timeout
	Transition to LP-RX

913 **Table 14 Sequence of Events for BTA Acknowledge Timeout (Host Processor initially TX)**

Host Processor Side	Peripheral Side
Host Processor in HS TX or LP TX mode	Peripheral in LP RX mode
Request Turnaround	
Turnaround Acknowledgement Timeout	(no change)
Return to <i>Stop</i> state (LP-11)	

914 **7.3.2 Peripheral Reset Timeout (PR\_TO)**

915 When a peripheral is reset, it requires a period of time before it is ready for normal operation. This timer is  
916 programmed with a value longer than the specified time required to complete the reset sequence. After it  
917 expires, the host may resume normal operation with the peripheral. The timeout value is peripheral-  
918 specific. This is an optional timer.

919 **Table 15 Sequence of Events for Peripheral Reset Timeout**

Host Processor Side	Peripheral Side
Send <i>Reset Entry</i> command	Receive <i>Reset Entry</i> Command
Return to <i>Stop</i> state (LP-11)	Initiate reset sequence
	Complete reset sequence

Host Processor Side	Peripheral Side
Peripheral Reset Timeout	
Resume Normal Operation.	Wait for bus activity

#### 920 **7.4 Acknowledge and Error Reporting Mechanism**

921 In a bidirectional Link, the peripheral monitors transmissions from the host processor using detection  
 922 features and timers specified in this section. Error information related to the transmission shall be stored in  
 923 the peripheral. Errors from multiple transmissions shall be stored and accumulated until a BTA following a  
 924 transmission provides the opportunity for the peripheral to report errors to the host processor.

925 The host processor may request a command acknowledge and error information related to any transmission  
 926 by asserting Bus Turnaround with the transmission. The peripheral shall respond with ACK Trigger  
 927 Message if there are no errors and with *Acknowledge and Error Report* packet if any errors were detected  
 928 in previous transmissions. Appropriate flags shall be set to indicate what errors were detected on the  
 929 preceding transmissions. If the transmission was a Read request, the peripheral shall return READ data  
 930 without issuing additional ACK Trigger Message or an *Acknowledge and Error Report* packet if no errors  
 931 were detected. If there was an error in the Read request, the peripheral shall return the appropriate  
 932 *Acknowledge and Error Report* unless the error was a single-bit correctable error. In that case, the  
 933 peripheral shall return the requested READ data packet followed by *Acknowledge and Error Report* packet  
 934 with appropriate error bits set.

935 Once errors are reported, the Error Register shall have all bits set to zero.

936 See section 8.10.1 for more detail on *Acknowledge and Error Report* protocols.

937

## 938 **8 DSI Protocol**

939 On the transmitter side of a DSI Link, parallel data, signal events, and commands are converted in the  
940 Protocol layer to packets, following the packet organization documented in this section. The Protocol layer  
941 appends packet-protocol information and headers, and then sends complete bytes through the Lane  
942 Management layer to the PHY. Packets are serialized by the PHY and sent across the serial Link. The  
943 receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into  
944 parallel data, signal events and commands.

945 If there are multiple Lanes, the Lane Management layer distributes bytes to separate PHYs, one PHY per  
946 Lane, as described in Section 6. Packet protocol and formats are independent of the number of Lanes used.

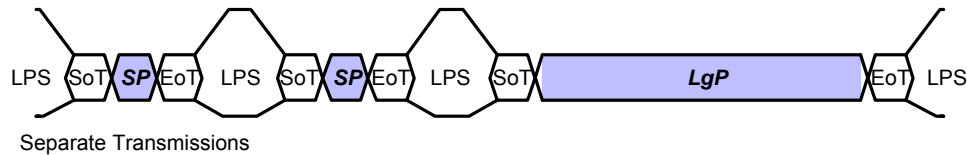
### 947 **8.1 Multiple Packets per Transmission**

948 In its simplest form, a transmission may contain one packet. If many packets are to be transmitted, the  
949 overhead of frequent switching between LPS and High-Speed Mode will severely limit bandwidth if  
950 packets are sent separately, e.g. one packet per transmission.

951 The DSI protocol permits multiple packets to be concatenated, which substantially boosts effective  
952 bandwidth. This is useful for events such as peripheral initialization, where many registers may be loaded  
953 with separate write commands at system startup.

954 There are two modes of data transmission, HS and LP transmission modes, at the PHY layer. Before a HS  
955 transmission can be started, the transmitter PHY issues a SoT sequence to the receiver. After that, data or  
956 command packets can be transmitted in HS mode. Multiple packets may exist within a single HS  
957 transmission and the end of transmission is always signaled at the PHY layer using a dedicated EoT  
958 sequence. In order to enhance the overall robustness of the system, DSI defines a dedicated EoT packet  
959 (EoTp) at the protocol layer (section 8.8.2) for signaling the end of HS transmission. For backwards  
960 compatibility with earlier DSI systems, the capability of generating and interpreting this EoTp can be  
961 enabled or disabled. The method of enabling or disabling this capability is out of scope for this document.  
962 PHY-based EoT and SoT sequences are defined in [MIPI04].

963 The top diagram in Figure 10 illustrates a case where multiple packets are being sent separately with EoTp  
964 support disabled. In HS mode, time gaps between packets shall result in separate HS transmissions for each  
965 packet, with a SoT, LPS, and EoT issued by the PHY layer between packets. This constraint does not apply  
966 to LP transmissions. The bottom diagram in Figure 10 demonstrates a case where multiple packets are  
967 concatenated within a single HS transmission.

**KEY:**

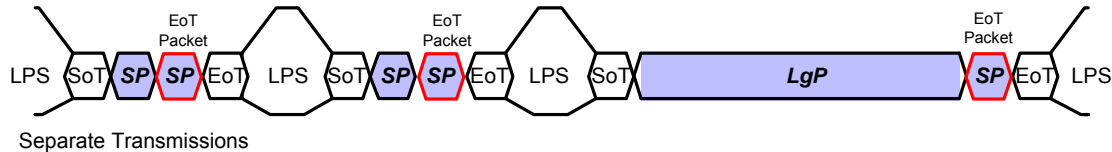
LPS – Low Power State  
 SoT – Start of Transmission  
 EoT – End of Transmission  
 SP – Short Packet  
 LgP – Long Packet

968

969

**Figure 10 HS Transmission Examples with EoTp disabled**

970 Figure 11 depicts HS transmission cases where EoTp generation is enabled. In the figure, EoT short  
 971 packets are highlighted in red. The top diagram illustrates a case where a host is intending to send a short  
 972 packet followed by a long packet using two separate transmissions. In this case, an additional EoT short  
 973 packet is generated before each transmission ends. This mechanism provides a more robust environment, at  
 974 the expense of increased overhead (four extra bytes per transmission) compared to cases where EoTp  
 975 generation is disabled, i.e. the system only relies on the PHY layer EoT sequence for signaling the end of  
 976 HS transmission. The overhead imposed by enabling EoTp can be minimized by sending multiple long and  
 977 short packets within a single transmission as illustrated by the bottom diagram in Figure 11.

**KEY:**

LPS – Low Power State  
 SoT – Start of Transmission  
 EoT – End of Transmission  
 SP – Short Packet  
 LgP – Long Packet

978

979

**Figure 11 HS Transmission Examples with EoTp enabled****8.2 Packet Composition**

981 The first byte of the packet, the Data Identifier (DI), includes information specifying the type of the packet.  
 982 For example, in Video Mode systems in a display application the logical unit for a packet may be one  
 983 horizontal display line. Command Mode systems send commands and an associated set of parameters, with  
 984 the number of parameters depending on the command type.



985 Packet sizes fall into two categories:

- 986 • **Short packets** are four bytes in length including the ECC. Short packets are used for most  
987 Command Mode commands and associated parameters. Other Short packets convey events like H  
988 Sync and V Sync edges. Because they are Short packets they can convey accurate timing  
989 information to logic at the peripheral.
- 990 • **Long packets** specify the payload length using a two-byte Word Count field. Payloads may be  
991 from 0 to  $2^{16} - 1$  bytes long. Therefore, a Long packet may be up to 65,541 bytes in length. Long  
992 packets permit transmission of large blocks of pixel or other data.

993 A special case of Command Mode operation is video-rate (update) streaming, which takes the form of an  
994 arbitrarily long stream of pixel or other data transmitted to the peripheral. As all DSI transactions use  
995 packets, the video stream shall be broken into separate packets. This “packetization” may be done by  
996 hardware or software. The peripheral may then reassemble the packets into a continuous video stream for  
997 display.

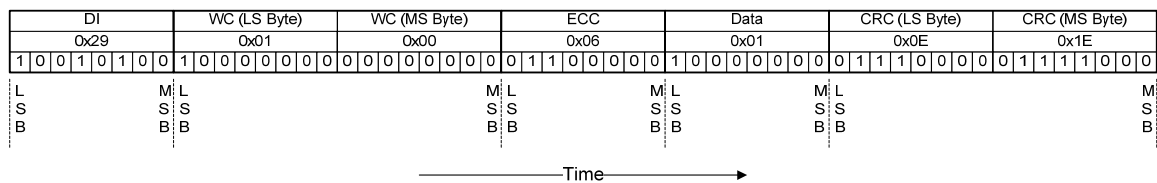
998 The *Set Maximum Return Packet Size* command allows the host processor to limit the size of response  
999 packets coming from a peripheral. See section 8.8.10 for a description of the command.

### 1000 8.3 Endian Policy

1001 All packet data traverses the interface as bytes. Sequentially, a transmitter shall send data LSB first, MSB  
1002 last. For packets with multi-byte fields, the least significant byte shall be transmitted first unless otherwise  
1003 specified.

1004 Figure 12 shows a complete Long packet data transmission. Note, the figure shows the byte values in  
1005 standard positional notation, i.e. MSB on the left and LSB on the right, while the bits are shown in  
1006 chronological order with the LSB on the left, the MSB on the right and time increasing left to right.

1007 See section 8.4.1 for a description of the Long packet format.



1008  
1009

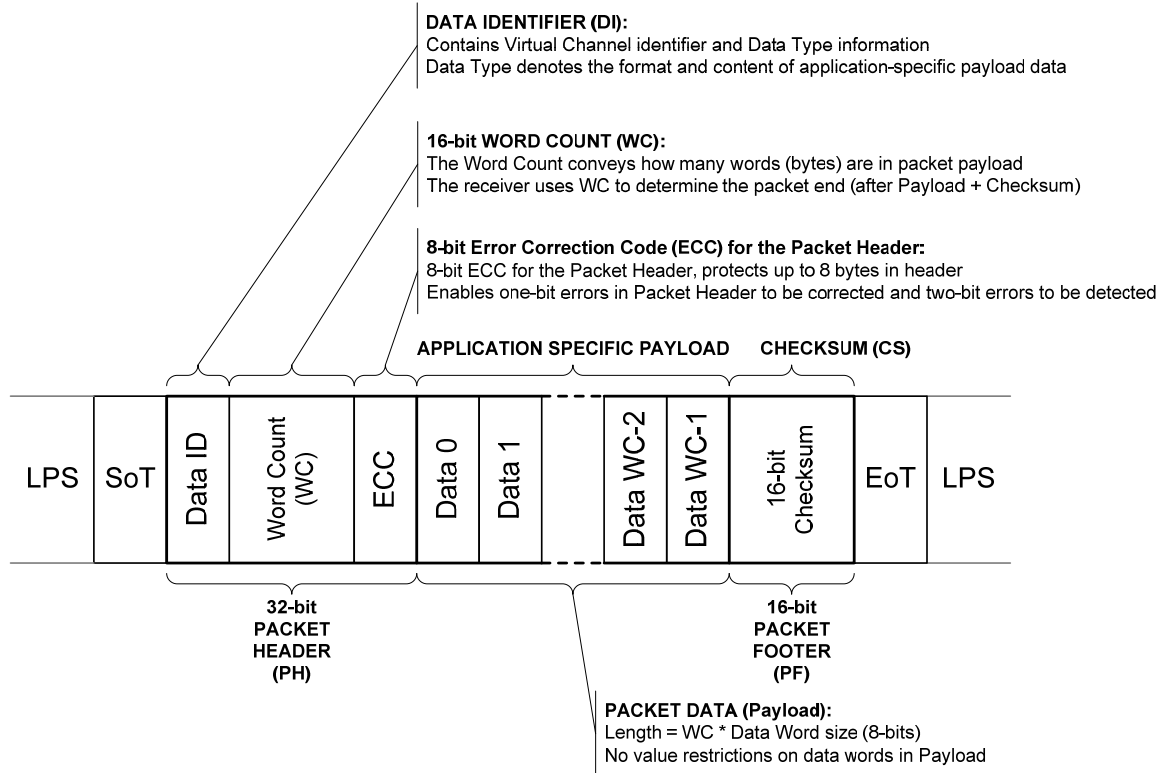
1010 **Figure 12 Endian Example (Long Packet)**

### 1011 8.4 General Packet Structure

1012 Two packet structures are defined for low-level protocol communication: Long packets and Short packets.  
1013 For both packet structures, the Data Identifier is always the first byte of the packet.

#### 1014 8.4.1 Long Packet Format

1015 Figure 13 shows the structure of the Long packet. A Long packet shall consist of three elements: a 32-bit  
1016 Packet Header (PH), an application-specific Data Payload with a variable number of bytes, and a 16-bit  
1017 Packet Footer (PF). The Packet Header is further composed of three elements: an 8-bit Data Identifier, a  
1018 16-bit Word Count, and 8-bit ECC. The Packet Footer has one element, a 16-bit checksum. Long packets  
1019 can be from 6 to 65,541 bytes in length.



1020  
1021

1022

**Figure 13 Long Packet Structure**

1023 The Data Identifier defines the Virtual Channel for the data and the Data Type for the application specific  
1024 payload data. See sections 8.8 through 8.10 for descriptions of Data Types.

1025 The Word Count defines the number of bytes in the Data Payload between the end of the Packet Header  
1026 and the start of the Packet Footer. Neither the Packet Header nor the Packet Footer shall be included in the  
1027 Word Count.

1028 The Error Correction Code (ECC) byte allows single-bit errors to be corrected and 2-bit errors to be  
1029 detected in the Packet Header. This includes both the Data Identifier and Word Count fields.

1030 After the end of the Packet Header, the receiver reads the next Word Count \* bytes of the Data Payload.  
1031 Within the Data Payload block, there are no limitations on the value of a data word, i.e. no embedded codes  
1032 are used.

1033 Once the receiver has read the Data Payload it reads the Checksum in the Packet Footer. The host processor  
1034 shall always calculate and transmit a Checksum in the Packet Footer. Peripherals are not required to  
1035 calculate a Checksum. Also note the special case of zero-byte Data Payload: if the payload has length 0,  
1036 then the Checksum calculation results in (0xFFFF). If the Checksum is not calculated, the Packet Footer  
1037 shall consist of two bytes of all zeros (0x0000). See section 9 for more information on calculating the  
1038 Checksum.

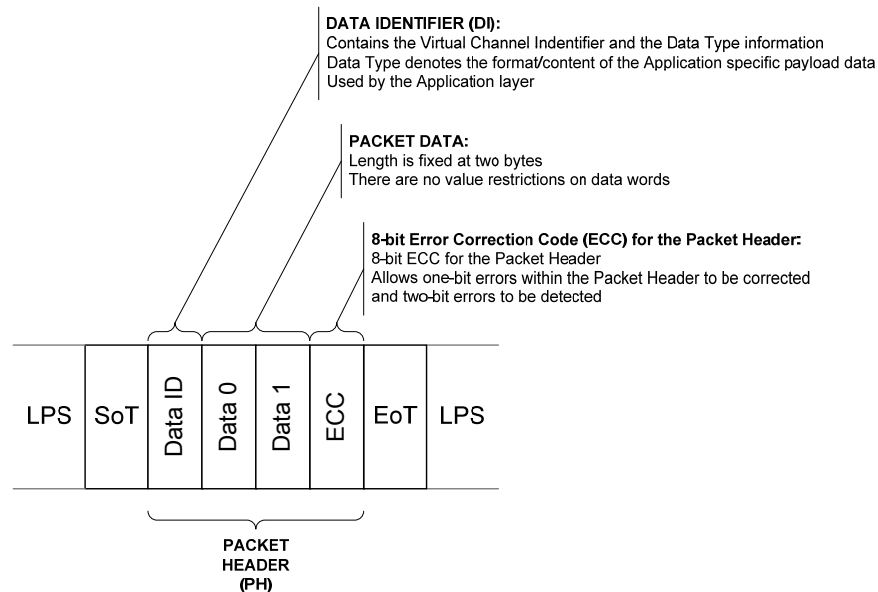
1039 In the generic case, the length of the Data Payload shall be a multiple of bytes. In addition, each data format  
1040 may impose additional restrictions on the length of the payload data, e.g. multiple of four bytes.

1041 Each byte shall be transmitted least significant bit first. Payload data may be transmitted in any byte order  
 1042 restricted only by data format requirements. Multi-byte elements such as Word Count and Checksum shall  
 1043 be transmitted least significant byte first.

#### 1044 **8.4.2 Short Packet Format**

1045 Figure 14 shows the structure of the Short packet. See sections 8.8 through 8.10 for descriptions of the Data  
 1046 Types. A Short packet shall contain an 8-bit Data ID followed by two command or data bytes and an 8-bit  
 1047 ECC; a Packet Footer shall not be present. Short packets shall be four bytes in length.

1048 The Error Correction Code (ECC) byte allows single-bit errors to be corrected and 2-bit errors to be  
 1049 detected in the Short packet.



1050

1051

**Figure 14 Short Packet Structure**

#### 1052 **8.5 Common Packet Elements**

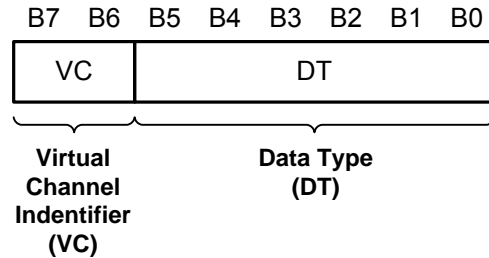
1053 Long and Short packets have several common elements that are described in this section.

##### 1054 **8.5.1 Data Identifier Byte**

1055 The first byte of any packet is the DI (Data Identifier) byte. Figure 15 shows the composition of the Data  
 1056 Identifier (DI) byte.

1057 DI[7:6]: These two bits identify the data as directed to one of four virtual channels.

1058 DI[5:0]: These six bits specify the Data Type.



1059

1060

**Figure 15 Data Identifier Byte**

### 1061 **8.5.1.1 Virtual Channel Identifier – VC field, DI[7:6]**

1062 A processor may service up to four peripherals with tagged commands or blocks of data, using the Virtual  
 1063 Channel ID field of the header for packets targeted at different peripherals.

1064 The Virtual Channel ID enables one serial stream to service two or more virtual peripherals by multiplexing  
 1065 packets onto a common transmission channel. Note that packets sent in a single transmission each have  
 1066 their own Virtual Channel assignment and can be directed to different peripherals. Although the DSI  
 1067 protocol permits communication with multiple peripherals, this specification only addresses the connection  
 1068 of a host processor to a single peripheral. Implementation details for connection to more than one physical  
 1069 peripheral are beyond the scope of this document.

### 1070 **8.5.1.2 Data Type Field DT[5:0]**

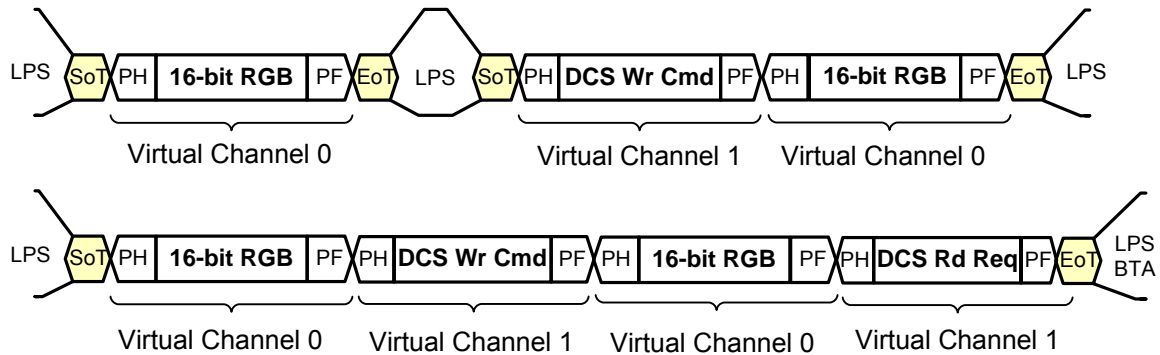
1071 The Data Type field specifies if the packet is a Long or Short packet type and the packet format. The Data  
 1072 Type field, along with the Word Count field for Long packets, informs the receiver of how many bytes to  
 1073 expect in the remainder of the packet. This is necessary because there are no special packet start / end sync  
 1074 codes to indicate the beginning and end of a packet. This permits packets to convey arbitrary data, but it  
 1075 also requires the packet header to explicitly specify the size of the packet.

1076 When the receiving logic has counted down to the end of a packet, it shall assume the next data is either the  
 1077 header of a new packet or the EoT (End of Transmission) sequence.

## 1078 **8.5.2 Error Correction Code**

1079 The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the  
 1080 Packet Header. The host processor shall always calculate and transmit an ECC byte. Peripherals shall  
 1081 support ECC in both forward- and reverse-direction communications. See section 9 for more information  
 1082 on coding and decoding the ECC and section 8.9.2 for ECC and Checksum requirements.

1083 **8.6 Interleaved Data Streams**



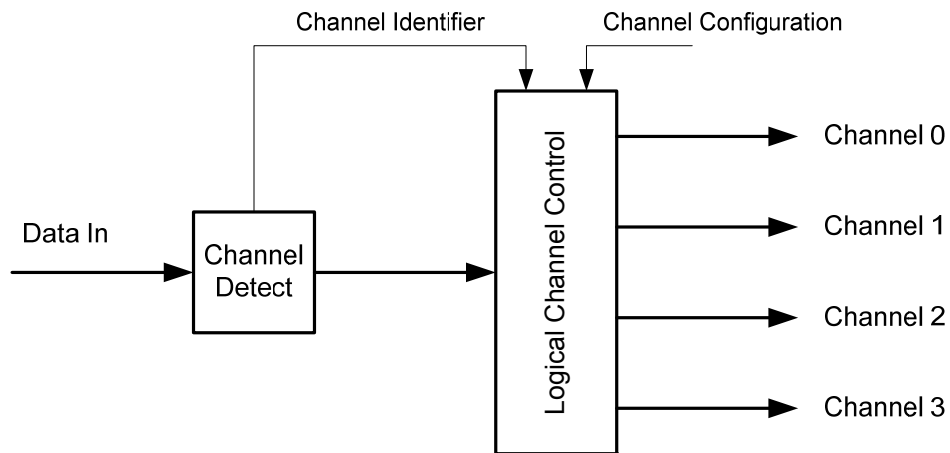
**KEY:**

- LPS – Low Power State
- SoT – Start of Transmission
- EoT – End of Transmission
- PH – Packet Header
- PF – Packet Footer
- BTA – Bus Turn-Around

1084  
1085

**Figure 16 Interleaved Data Stream Example with EoTp disabled**

1086 One application for multiple channels is a high-resolution display using two or more separate driver ICs on  
 1087 a single display module. Each driver IC addresses only a portion of the columns on the display device.  
 1088 Each driver IC captures and displays only the packet contents targeted for that driver and ignores the other  
 1089 packets. See Figure 17.



1090  
1091

**Figure 17 Logical Channel Block Diagram (Receiver Case)**

1092 **8.6.1 Interleaved Data Streams and Bidirectionality**

1093 When multiple peripherals have bidirectional capability there shall be a clear and unambiguous means for  
 1094 returning READ data, events and status back to the host processor from the intended peripheral. The  
 1095 combination of BTA and the Virtual Channel ID ensures no confusion over which peripheral is expected to  
 1096 respond to any request from the peripheral. Returning packets shall be tagged with the ID of the peripheral  
 1097 that sent the packet.

1098 A consequence of bidirectionality is any transmission from the host processor shall contain no more than  
 1099 one packet requiring a peripheral response. This applies regardless of the number of peripherals that may be  
 1100 connected via the Link to the host processor.

## 1101 8.7 Processor to Peripheral Direction (Processor-Sourced) Packet Data Types

1102 The set of transaction types sent from the host processor to a peripheral, such as a display module, are  
 1103 shown in Table 16.

1104 **Table 16 Data Types for Processor-sourced Packets**

Data Type, hex	Data Type, binary	Description	Packet Size
0x01	00 0001	Sync Event, V Sync Start	Short
0x11	01 0001	Sync Event, V Sync End	Short
0x21	10 0001	Sync Event, H Sync Start	Short
0x31	11 0001	Sync Event, H Sync End	Short
0x08	00 1000	End of Transmission packet (EoTp)	Short
0x02	00 0010	Color Mode (CM) Off Command	Short
0x12	01 0010	Color Mode (CM) On Command	Short
0x22	10 0010	Shut Down Peripheral Command	Short
0x32	11 0010	Turn On Peripheral Command	Short
0x03	00 0011	Generic Short WRITE, no parameters	Short
0x13	01 0011	Generic Short WRITE, 1 parameter	Short
0x23	10 0011	Generic Short WRITE, 2 parameters	Short
0x04	00 0100	Generic READ, no parameters	Short
0x14	01 0100	Generic READ, 1 parameter	Short
0x24	10 0100	Generic READ, 2 parameters	Short
0x05	00 0101	DCS Short WRITE, no parameters	Short
0x15	01 0101	DCS Short WRITE, 1 parameter	Short
0x06	00 0110	DCS READ, no parameters	Short
0x37	11 0111	Set Maximum Return Packet Size	Short
0x09	00 1001	Null Packet, no data	Long
0x19	01 1001	Blanking Packet, no data	Long
0x29	10 1001	Generic Long Write	Long
0x39	11 1001	DCS Long Write/write_LUT Command Packet	Long
0x0C	00 1100	Loosely Packed Pixel Stream, 20-bit YCbCr, 4:2:2 Format	Long
0x1C	01 1100	Packed Pixel Stream, 24-bit YCbCr, 4:2:2 Format	Long
0x2C	10 1100	Packed Pixel Stream, 16-bit YCbCr, 4:2:2 Format	Long
0x0D	00 1101	Packed Pixel Stream, 30-bit RGB, 10-10-10 Format	Long
0x1D	01 1101	Packed Pixel Stream, 36-bit RGB, 12-12-12 Format	Long

Data Type, hex	Data Type, binary	Description	Packet Size
0x3D	11 1101	Packed Pixel Stream, 12-bit YCbCr, 4:2:0 Format	Long
0x0E	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
0x1E	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
0x2E	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
0x3E	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long
0xX0 and 0xXF, unspecified	XX 0000 XX 1111	DO NOT USE All unspecified codes are reserved	

## 1105 8.8 Processor-to-Peripheral Transactions – Detailed Format Description

### 1106 8.8.1 Sync Event (H Start, H End, V Start, V End), Data Type = XX 0001 (0xX1)

1107 Sync Events are Short packets and, therefore, can time-accurately represent events like the start and end of  
 1108 sync pulses. As “start” and “end” are separate and distinct events, the length of sync pulses, as well as  
 1109 position relative to active pixel data, e.g. front and back porch display timing, may be accurately conveyed  
 1110 to the peripheral. The Sync Events are defined as follows:

- 1111 • Data Type = 00 0001 (0x01) V Sync Start
- 1112 • Data Type = 01 0001 (0x11) V Sync End
- 1113 • Data Type = 10 0001 (0x21) H Sync Start
- 1114 • Data Type = 11 0001 (0x31) H Sync End

1115 In order to represent timing information as accurately as possible a V Sync Start event represents the start  
 1116 of the VSA and also implies an H Sync Start event for the first line of the VSA. Similarly, a V Sync End  
 1117 event implies an H Sync Start event for the last line of the VSA. If the host processor sources interlaced  
 1118 video, horizontal sync timing follows standard interlaced video conventions for the video format being used  
 1119 and are beyond the scope of this specification. See [CEA01] for timing details of interlaced video formats.  
 1120 The first field of interlaced video follows the same rules to imply H Sync Start. The peripheral (display),  
 1121 when receiving the interlaced second video field, shall not imply an H Sync Start at the V Sync Start and V  
 1122 Sync End timing. Refer to Annex C for a detailed progression order of event packets for progressive scan  
 1123 and interlaced scan video timing.

1124 Sync events should occur in pairs, Sync Start and Sync End, if accurate pulse-length information needs to  
 1125 be conveyed. Alternatively, if only a single point (event) in time is required, a single sync event (normally,  
 1126 Sync Start) may be transmitted to the peripheral. Sync events may be concatenated with blanking packets to  
 1127 convey inter-line timing accurately and avoid the overhead of switching between LPS and HS for every  
 1128 event. Note there is a power penalty for keeping the data line in HS mode, however.

1129 Display modules that do not need traditional sync/blanking/pixel timing should transmit pixel data in a  
 1130 high-speed burst then put the bus in Low Power Mode, for reduced power consumption. The recommended  
 1131 burst size is a scan line of pixels, which may be temporarily stored in a line buffer on the display module.

### 1132 8.8.2 EoTp, Data Type = 00 1000 (0x08)

1133 This short packet is used for indicating the end of a HS transmission to the data link layer. As a result,  
 1134 detection of the end of HS transmission may be decoupled from physical layer characteristics. [MIPI04]

1135 defines an EoT sequence composed of a series of all 1's or 0's depending on the last bit of the last packet  
 1136 within a HS transmission. Due to potential errors, the EoT sequence could be interpreted incorrectly as  
 1137 valid data types. Although EoT errors are not expected to happen frequently, the addition of this packet will  
 1138 enhance overall system reliability.

1139 Devices compliant to earlier revisions of the DSI specification do not support EoTp generation or detection.  
 1140 A Host or peripheral device compliant to this revision of DSI specification shall incorporate capability of  
 1141 supporting EoTp. The device shall also provide an implementation-specific means for enabling and  
 1142 disabling this capability to ensure interoperability with earlier DSI devices that do not support the EoTp.

1143 The main objective of the EoTp is to enhance overall robustness of the system during HS transmission  
 1144 mode. Therefore, DSI transmitters should not generate an EoTp when transmitting in LP mode. The Data  
 1145 Link layer of DSI receivers shall detect and interpret arriving EoTps regardless of transmission mode (HS  
 1146 or LP modes) in order to decouple itself from the physical layer. Table 17 describes how DSI mandates  
 1147 EoTp support for different transmission and reception modes.

1148 **Table 17 EoT Support for Host and Peripheral**

DSI Host (EoT capability enabled)				DSI Peripheral (EoT capability enabled)			
HS Mode		LP Mode		HS Mode		LP Mode	
Receive	Transmit	Receive	Transmit	Receive	Transmit	Receive	Transmit
Not Applicable	"Shall"	"Shall"	"Should not"	"Shall"	Not Applicable	"Shall"	"Should not"

1149 Unlike other DSI packets, an EoTp has a fixed format as follows:

- 1150 • Data Type = DI [5:0] = 0b001000
- 1151 • Virtual Channel = DI [7:6] = 0b00
- 1152 • Payload Data [15:0] = 0x0F0F
- 1153 • ECC [7:0] = 0x01

1154 The virtual channel identifier associated with an EoTp is fixed to 0, regardless of the number of different  
 1155 virtual channels present within the same transmission. For multi-Lane systems, the EoTp bytes are  
 1156 distributed across multiple Lanes.

### 1157 **8.8.3 Color Mode Off Command, Data Type = 00 0010 (0x02)**

1158 *Color Mode Off* is a Short packet command that returns a Video Mode display module from low-color  
 1159 mode to normal display operation.

### 1160 **8.8.4 Color Mode On Command, Data Type = 01 0010 (0x12)**

1161 *Color Mode On* is a Short packet command that switches a Video Mode display module to a low-color  
 1162 mode for power saving.



1163 **8.8.5 Shutdown Peripheral Command, Data Type = 10 0010 (0x22)**

1164 *Shutdown Peripheral* command is a Short packet command that turns off the display in a Video Mode  
1165 display module for power saving. Note the interface shall remain powered in order to receive the turn-on,  
1166 or wake-up, command.

1167 **8.8.6 Turn On Peripheral Command, Data Type = 11 0010 (0x32)**

1168 *Turn On Peripheral* command is Short packet command that turns on the display in a Video Mode display  
1169 module for normal display operation.

1170 **8.8.7 Generic Short WRITE Packet with 0, 1, or 2 parameters, Data Types = 00  
1171 0011 (0x03), 01 0011 (0x13), 10 0011 (0x23), Respectively**

1172 *Generic Short WRITE* command is a Short packet type for sending generic data to the peripheral. The  
1173 format and interpretation of the contents of this packet are outside the scope of this document. It is the  
1174 responsibility of the system designer to ensure that both the host processor and peripheral agree on the  
1175 format and interpretation of such data.

1176 The complete packet shall be four bytes in length including an ECC byte. The two Data Type MSBs, bits  
1177 [5:4], indicate the number of valid parameters (0, 1, or 2). For single-byte parameters, the parameter shall  
1178 be sent in the first data byte following the DI byte and the second data byte shall be set to 0x00.

1179 **8.8.8 Generic READ Request with 0, 1, or 2 Parameters, Data Types = 00 0100  
1180 (0x04), 01 0100 (0x14), 10 0100(0x24), Respectively**

1181 *Generic READ* request is a Short packet requesting data from the peripheral. The format and interpretation  
1182 of the parameters of this packet, and of returned data, are outside the scope of this document. It is the  
1183 responsibility of the system designer to ensure that both the host processor and peripheral agree on the  
1184 format and interpretation of such data.

1185 Returned data may be of Short or Long packet format. Note the *Set Max Return Packet Size* command  
1186 limits the size of returning packets so that the host processor can prevent buffer overflow conditions when  
1187 receiving data from the peripheral. If the returning block of data is larger than the maximum return packet  
1188 size specified, the read response will require more than one transmission. The host processor shall send  
1189 multiple Generic READ requests in separate transmissions if the requested data block is larger than the  
1190 maximum packet size.

1191 The complete packet shall be four bytes in length including an ECC byte. The two Data Type MSBs, bits  
1192 [5:4], indicate the number of valid parameters (0, 1, or 2). For single byte parameters, the parameter shall  
1193 be sent in the first data byte following the DI byte and the second data byte shall be set to 0x00.

1194 Since this is a read command, BTA shall be asserted by the host processor following this request.

1195 The peripheral shall respond to Generic READ Request in one of the following ways:

- 1196 • If an error was detected by the peripheral, it shall send *Acknowledge and Error Report*. If an ECC  
1197 error in the request was detected and corrected, the peripheral shall transmit the requested READ  
1198 data packet with the *Acknowledge and Error Report* packet appended, in the same transmission.
- 1199 • If no error was detected by the peripheral, it shall send the requested READ packet (Short or  
1200 Long) with appropriate ECC and Checksum, if Checksum is enabled.

1201 A Generic READ request shall be the only, or last, packet of a transmission. Following the transmission the  
 1202 host processor sends BTA. Having given control of the bus to the peripheral, the host processor will expect  
 1203 the peripheral to transmit the appropriate response packet and then return bus possession to the host  
 1204 processor.

### 1205 **8.8.9 DCS Commands**

1206 DCS is a standardized command set intended for Command Mode display modules. The interpretation of  
 1207 DCS commands is supplied in [MIPI01].

1208 For DCS short commands, the first byte following the Data Identifier Byte is the *DCS Command Byte*. If  
 1209 the DCS command does not require parameters, the second payload byte shall be 0x00.

1210 If a DCS Command requires more than one parameter, the command shall be sent as a Long Packet type.

#### 1211 **8.8.9.1 DCS Short Write Command, 0 or 1 parameter, Data Types = 00 0101 (0x05), 01** 1212 **0101 (0x15), Respectively**

1213 *DCS Short Write* command is used to write a single data byte to a peripheral such as a display module. The  
 1214 packet is a Short packet composed of a Data ID byte, a DCS Write command, an optional parameter byte  
 1215 and an ECC byte. Data Type bit 4 shall be set to 1 if there is a valid parameter byte, and shall be set to 0 if  
 1216 there is no valid parameter byte. If a parameter is not required, the parameter byte shall be 0x00. If *DCS*  
 1217 *Short Write* command, followed by BTA, is sent to a bidirectional peripheral, the peripheral shall respond  
 1218 with ACK Trigger Message unless an error was detected in the host-to-peripheral transmission. If the  
 1219 peripheral detects an error in the transmission, the peripheral shall respond with *Acknowledge and Error*  
 1220 *Report*. If the peripheral is a Video Mode display on a unidirectional DSI, it shall ignore BTA. See Table  
 1221 19.

#### 1222 **8.8.9.2 DCS Read Request, No Parameters, Data Type = 00 0110 (0x06)**

1223 DCS READ commands are used to request data from a display module. This packet is a Short packet  
 1224 composed of a Data ID byte, a DCS Read command, a byte set to 0x00 and an ECC byte. Since this is a  
 1225 read command, BTA shall be asserted by the host processor following completion of the transmission.  
 1226 Depending on the type of READ requested in the DCS Command Byte, the peripheral may respond with a  
 1227 DCS Short Read Response or DCS Long Read Response.

1228 The read response may be more than one packet in the case of DCS Long Read Response, if the returning  
 1229 block of data is larger than the maximum return packet size specified. In that case, the host processor shall  
 1230 send multiple DCS Read Request commands to transfer the complete data block. See section 8.8.10 for  
 1231 details on setting the read packet size.

1232 The peripheral shall respond to DCS READ Request in one of the following ways:

- 1233 • If an error was detected by the peripheral, it shall send *Acknowledge and Error Report*. If an ECC  
 1234 error in the request was detected and corrected, the peripheral shall send the requested READ data  
 1235 packet followed by the *Acknowledge and Error Report* packet in the same transmission.
- 1236 • If no error was detected by the peripheral, it shall send the requested READ packet (Short or  
 1237 Long) with appropriate ECC and Checksum, if either or both features are enabled.

1238 A DCS Read Request packet shall be the only, or last, packet of a transmission. Following the transmission,  
 1239 the host processor sends BTA. Having given control of the bus to the peripheral, the host processor will  
 1240 expect the peripheral to transmit the appropriate response packet and then return bus possession to the host  
 1241 processor.

1242 **8.8.9.3 DCS Long Write / write\_LUT Command, Data Type = 11 1001 (0x39)**

1243 *DCS Long Write/write\_LUT Command* is used to send larger blocks of data to a display module that  
1244 implements the Display Command Set.

1245 The packet consists of the DI byte, a two-byte WC, an ECC byte, followed by the *DCS Command Byte*, a  
1246 payload of length WC minus one bytes, and a two-byte checksum.

1247 **8.8.10 Set Maximum Return Packet Size, Data Type = 11 0111 (0x37)**

1248 *Set Maximum Return Packet Size* is a four-byte command packet (including ECC) that specifies the  
1249 maximum size of the payload in a Long packet transmitted from peripheral back to the host processor. The  
1250 order of bytes in *Set Maximum Return Packet Size* is: Data ID, two-byte value for maximum return packet  
1251 size, followed by the ECC byte. Note that the two-byte value is transmitted with LS byte first. This  
1252 command shall be ignored by peripherals with unidirectional DSI interfaces.

1253 During a power-on or Reset sequence, the Maximum Return Packet Size shall be set by the peripheral to a  
1254 default value of one. This parameter should be set by the host processor to the desired value in the  
1255 initialization routine before commencing normal operation.

1256 **8.8.11 Null Packet (Long), Data Type = 00 1001 (0x09)**

1257 *Null Packet* is a mechanism for keeping the serial Data Lane(s) in High-Speed mode while sending dummy  
1258 data. This is a Long packet. Like all packets, its content shall be an integer number of bytes.

1259 The Null Packet consists of the DI byte, a two-byte WC, ECC byte, and “null” payload of WC bytes,  
1260 ending with a two-byte Checksum. Actual data values sent are irrelevant because the peripheral does not  
1261 capture or store the data. However, ECC and Checksum shall be generated and transmitted to the  
1262 peripheral.

1263 **8.8.12 Blanking Packet (Long), Data Type = 01 1001 (0x19)**

1264 A Blanking packet is used to convey blanking timing information in a Long packet. Normally, the packet  
1265 represents a period between active scan lines of a Video Mode display, where traditional display timing is  
1266 provided from the host processor to the display module. The blanking period may have *Sync Event* packets  
1267 interspersed between blanking segments. Like all packets, the Blanking packet contents shall be an integer  
1268 number of bytes. Blanking packets may contain arbitrary data as payload.

1269 The Blanking packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes,  
1270 and a two-byte checksum.

1271 **8.8.13 Generic Long Write, Data Type = 10 1001 (0x29)**

1272 *Generic Long Write Packet* is used to transmit arbitrary blocks of data from a host processor to a peripheral  
1273 in a Long packet. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC  
1274 bytes and a two-byte checksum.

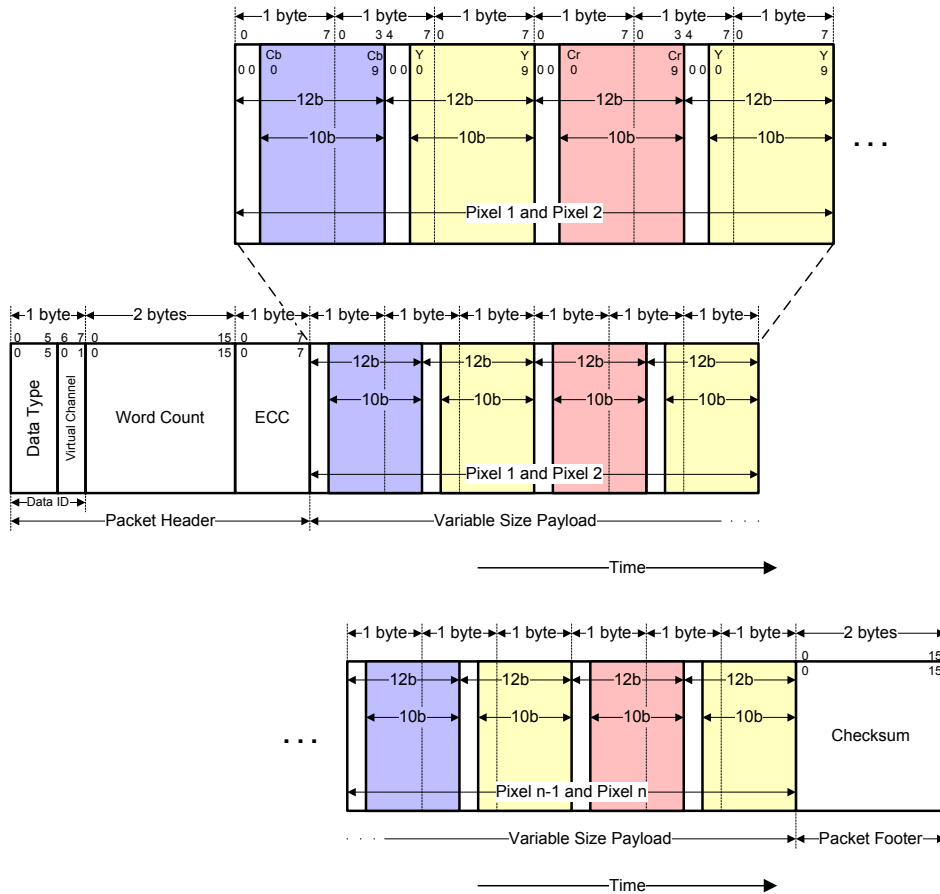
1275 **8.8.14 Loosely Packed Pixel Stream, 20-bit YCbCr 4:2:2 Format, Data Type = 00  
1276 1100 (0x0C)**

1277 *Loosely Packed Pixel Stream 20-bit YCbCr 4:2:2 Format* shown in Figure 18 is a Long packet used to  
1278 transmit image data formatted as 20-bits per pixel to a Video Mode display module. The packet consists of

1279 the DI byte, a two-byte, non-zero WC, an ECC byte, a payload of length WC bytes and a two-byte  
 1280 Checksum.

1281 When transmitting standard definition video, e.g. NTSC 480i30 or PAL 525i25, the pixel format is ITU-R  
 1282 Recommendation BT.601 (see [ITU01]). When transmitting high definition video, e.g. 1080i25, 1080i30 or  
 1283 720p60, the pixel format is ITU-R Recommendation BT.709 (see [ITU02]). Component ordering follows  
 1284 ITU-R Recommendation BT.656 (see [ITU03]).

1285 A pixel shall have ten bits for each of the Y-, Cb-, and Cr-components loosely packed into 12-bit fields as  
 1286 shown in Figure 18. The 10-bit component value shall be justified such that the most significant bits of the  
 1287 12-bit field, b[11:2] holds the 10-bit component value, d[9:0]. The least significant bits of the 12-bit field,  
 1288 b[1:0], shall be 00b. Within a component, the LSB is sent first, the MSB last.



1289

1290

**Figure 18 20-bit per Pixel – YCbCr 4:2:2 Format, Long Packet**

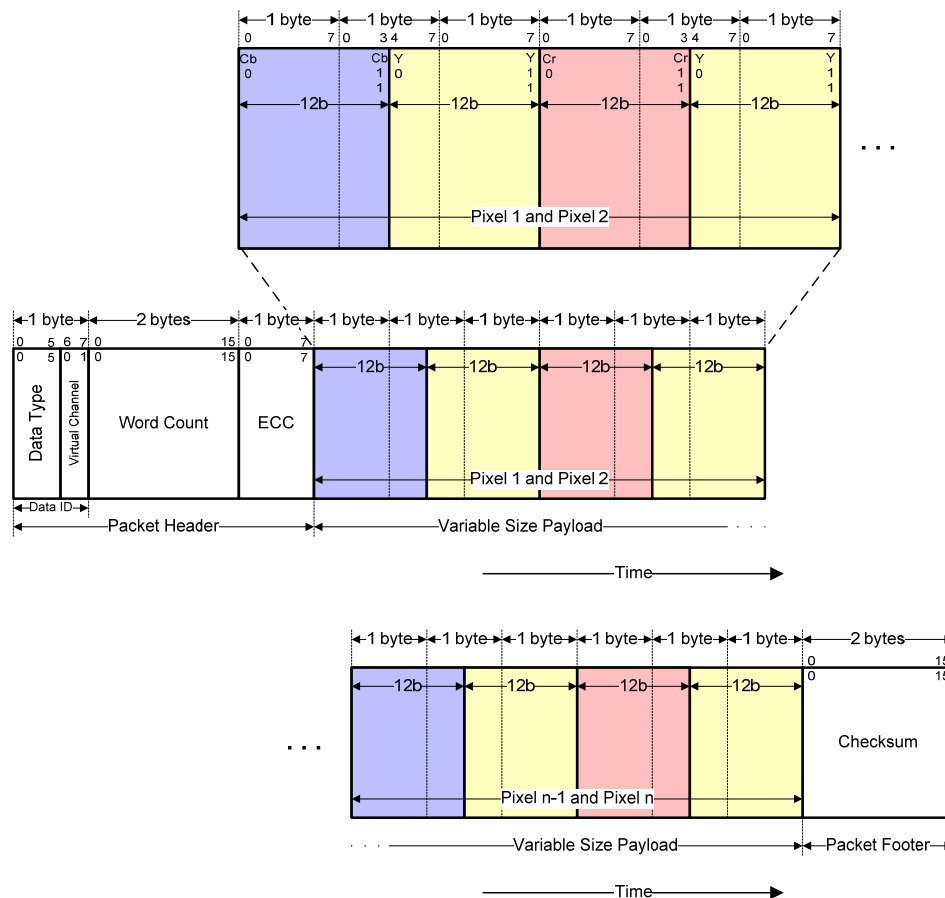
1291 With this format, pixel boundaries align with certain byte boundaries. The value in WC (size of payload in  
 1292 bytes) shall be any non-zero value divisible into an integer by six. Allowable values for WC = {6, 12, 18,...  
 1293 65 532}.

1294 **8.8.15 Packed Pixel Stream, 24-bit YCbCr 4:2:2 Format, Data Type = 01 1100**  
 1295 **(0x1C)**

1296 *Packed Pixel Stream 24-bit YCbCr 4:2:2 Format* shown in Figure 19 is a Long packet used to transmit  
 1297 image data formatted as 24-bits per pixel to a Video Mode display module. The packet consists of the DI  
 1298 byte, a two-byte, non-zero WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum.

1299 When transmitting standard definition video, e.g. NTSC 480i30 or PAL 525i25, the pixel format is ITU-R  
 1300 Recommendation BT.601 (see [ITU01]). When transmitting high definition video, e.g. 1080i25, 1080i30 or  
 1301 720p60, the pixel format is ITU-R Recommendation BT.709 (see [ITU02]). Component ordering follows  
 1302 ITU-R Recommendation BT.656 (see [ITU03]).

1303 A pixel shall have twelve bits for each of the Y-, Cb-, and Cr-components as shown in Figure 19. Within a  
 1304 component, the LSB is sent first, the MSB last.



1305

1306

**Figure 19 24-bit per Pixel – YCbCr 4:2:2 Format, Long Packet**

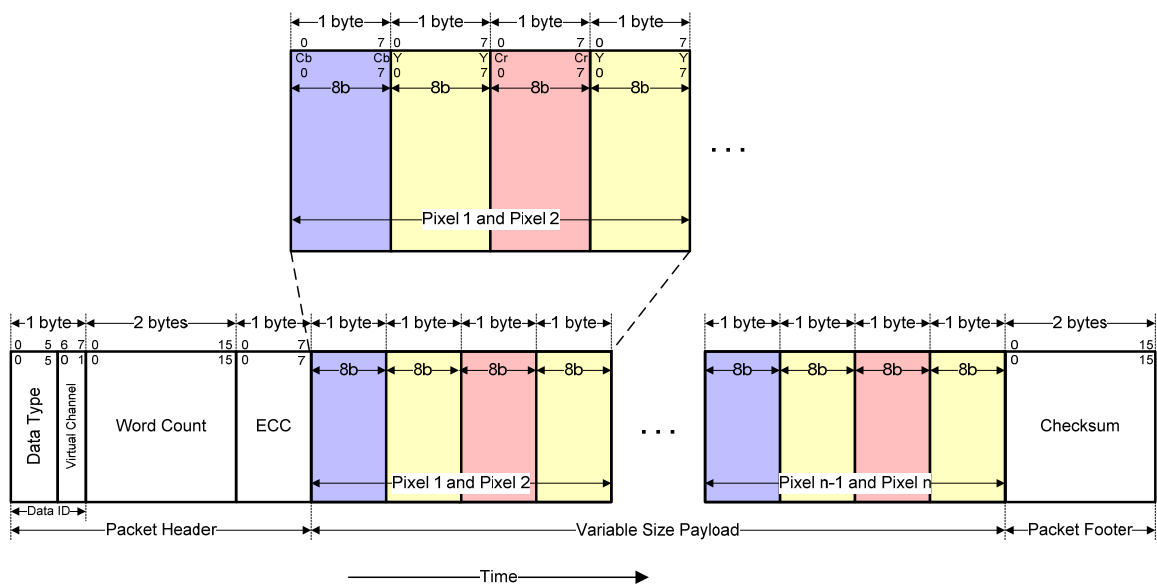
1307 With this format, pixel boundaries align with certain byte boundaries. The value in WC (size of payload in  
 1308 bytes) shall be any non-zero value divisible into an integer by six. Allowable values for WC = {6, 12, 18,...  
 1309 65 532}.

1310 **8.8.16 Packed Pixel Stream, 16-bit YCbCr 4:2:2 Format, Data Type = 10 1100**  
 1311 **(0x2C)**

1312 *Packed Pixel Stream 16-bit YCbCr 4:2:2 Format* shown in Figure 20 is a Long packet used to transmit  
 1313 image data formatted as 16-bits per pixel to a Video Mode display module. The packet consists of the DI  
 1314 byte, a two-byte, non-zero WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum.

1315 When transmitting standard definition video, e.g. NTSC 480i30 or PAL 525i25, the pixel format is ITU-R  
 1316 Recommendation BT.601 (see [ITU01]). When transmitting high definition video, e.g. 1080i25, 1080i30 or  
 1317 720p60, the pixel format is ITU-R Recommendation BT.709 (see [ITU02]). Component ordering follows  
 1318 ITU-R Recommendation BT.656 (see [ITU03]).

1319 A pixel shall have eight bits for each of the Y-, Cb-, and Cr-components. Within a component, the LSB is  
 1320 sent first, the MSB last.



1321

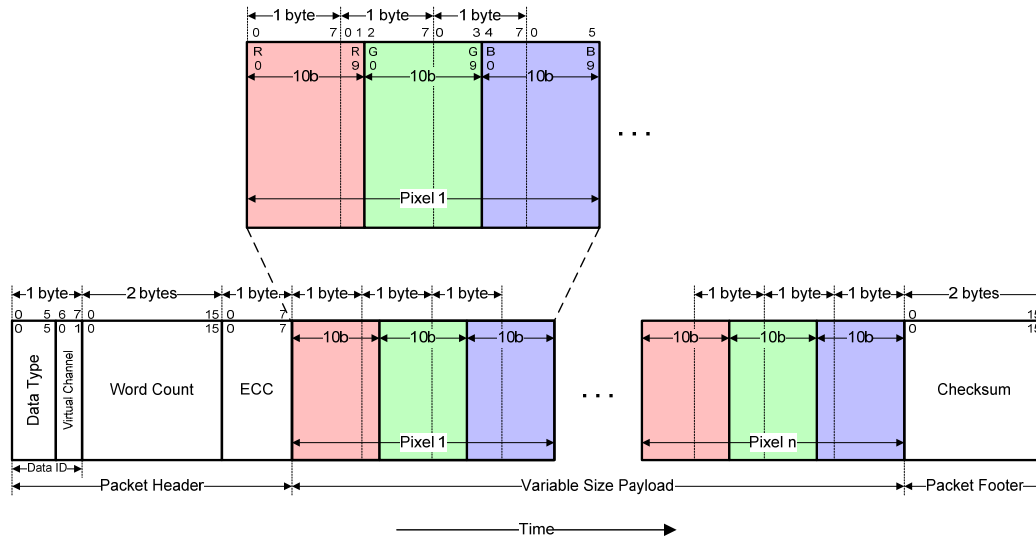
1322

**Figure 20 16-bit per Pixel – YCbCr 4:2:2 Format, Long Packet**

1323 With this format, pixel boundaries align with certain byte boundaries. The value in WC (size of payload in  
 1324 bytes) shall be any non-zero value divisible into an integer by four. Allowable values for WC = {4, 8, 12,...  
 1325 65 532}.

1326 **8.8.17 Packed Pixel Stream, 30-bit Format, Long Packet, Data Type = 00 1101**  
 1327 **(0x0D)**

1328 *Packed Pixel Stream 30-Bit Format* shown in Figure 21 is a Long packet used to transmit image data  
 1329 formatted as 30-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte,  
 1330 non-zero WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is  
 1331 red (10 bits), green (10 bits) and blue (10 bits), in that order. Within a color component, the LSB is sent  
 1332 first, the MSB last.



1333

1334

**Figure 21 30-bit per Pixel (Packed) – RGB Color Format, Long Packet**

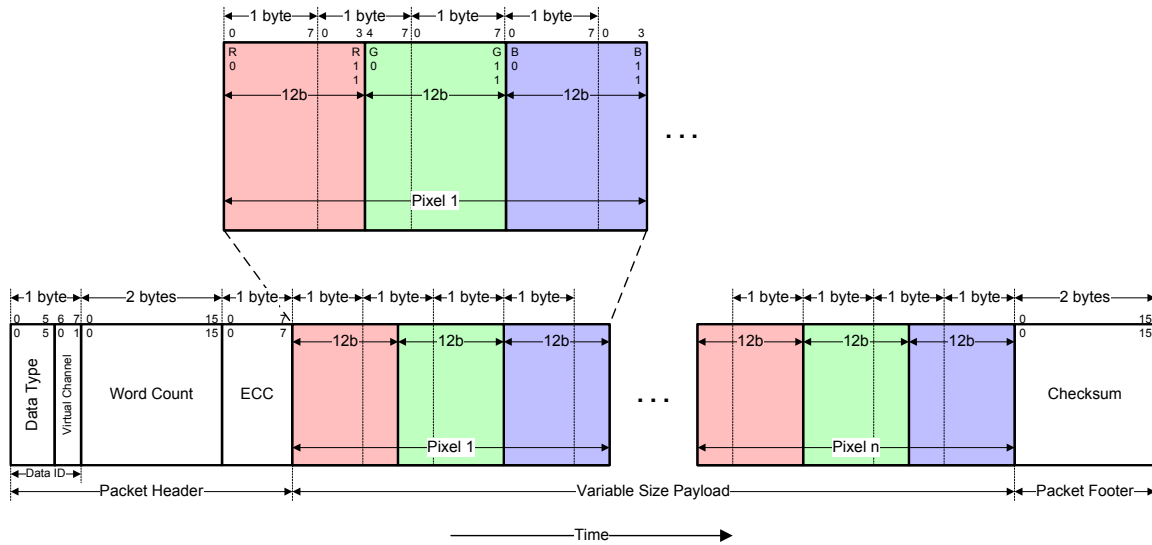
1335 This format uses sRGB color space. However, this Data Type may apply to other color spaces or data  
 1336 transfers using 30-bits per pixel when the color space, or related formatting information, is explicitly  
 1337 defined by a prior display command. For example, a future revision of [MIPI01] may extend the Data Type  
 1338 to include color spaces that differ from sRGB. The scope and nature of the formatting command is outside  
 1339 the scope of this document.

1340 With this format, pixel boundaries align with byte boundaries every four pixels (fifteen bytes). The total  
 1341 line width (displayed plus non-displayed pixels) should be a multiple of fifteen bytes. However, the value  
 1342 in WC (size of payload in bytes) shall not be restricted to non-zero values divisible by fifteen.

1343 Any trailing bits within a byte not entirely used by pixel data shall be zero. For example, a packet with only  
 1344 one pixel requires two trailing zero bits in the fourth data byte. If the pixel RGB value is 0b1111111111  
 1345 1111111111 1111111111, the fourth byte value equals 0x3F. The entire packet with VC = 0b00 would be  
 1346 0x0D 01 00 1E FF FF FF 3F B4 36.

#### 1347 **8.8.18 Packed Pixel Stream, 36-bit Format, Long Packet, Data Type = 01 1101** 1348 **(0x1D)**

1349 *Packed Pixel Stream 36-Bit Format* shown in Figure 22 is a Long packet used to transmit image data  
 1350 formatted as 36-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte,  
 1351 non-zero WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is  
 1352 red (12 bits), green (12 bits) and blue (12 bits), in that order. Within a color component, the LSB is sent  
 1353 first, the MSB last.



1354

1355

**Figure 22 36-bit per Pixel (Packed) – RGB Color Format, Long Packet**

1356 This format uses sRGB color space. However, this Data Type may apply to other color spaces or data  
 1357 transfers using 36-bits per pixel when the color space, or related formatting information, is explicitly  
 1358 defined by a prior display command. For example, a future revision of [MIPI01] may extend the Data Type  
 1359 to include color spaces that differ from sRGB. The scope and nature of the formatting command is outside  
 1360 the scope of this document.

1361 With this format, pixel boundaries align with byte boundaries every two pixels (nine bytes). The total line  
 1362 width (displayed plus non-displayed pixels) should be a multiple of nine bytes. However, the value in WC  
 1363 (size of payload in bytes) shall not be restricted to non-zero values divisible by nine.

1364 Any trailing bits within a byte not entirely used by pixel data shall be zero. For example, a packet with only  
 1365 one pixel requires four trailing zero bits in the fifth payload byte. If the pixel RGB value is  
 1366 0b111111111111 111111111111 111111111111, the fifth byte value equals 0x0F. The entire packet with  
 1367 VC = 0b00 would be 0x1D 01 00 0D FF FF FF FF 0F 4C 1C.

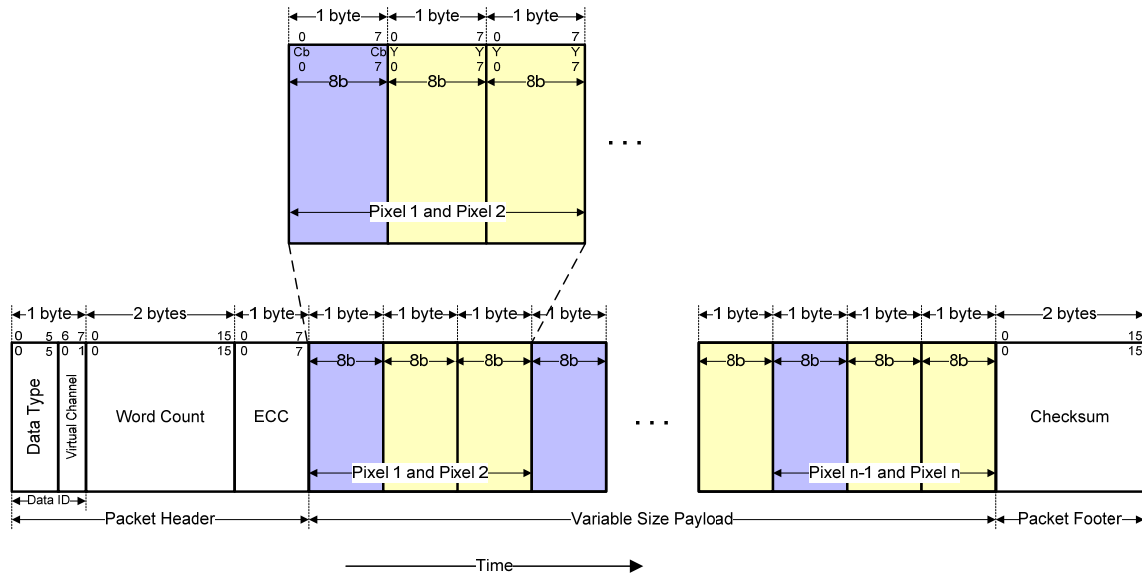
### 1368 **8.8.19 Packed Pixel Stream, 12-bit YCbCr 4:2:0 Format, Data Type = 11 1101** 1369 **(0x3D)**

1370 *Packed Pixel Stream 12-bit YCbCr 4:2:0 Format* shown in Figure 23 and Figure 24 is a Long packet used  
 1371 to transmit image data formatted as 12-bits per pixel to a Video Mode display module. The packet consists  
 1372 of the DI byte, a two-byte, non-zero WC, an ECC byte, a payload of length WC bytes and a two-byte  
 1373 Checksum.

1374 When transmitting standard definition video, e.g. NTSC 480i30 or PAL 525i25, the pixel format is ITU-R  
 1375 Recommendation BT.601 (see [ITU01]). When transmitting high definition video, e.g. 1080i25, 1080i30 or  
 1376 720p60, the pixel format is ITU-R Recommendation BT.709 (see [ITU02]).

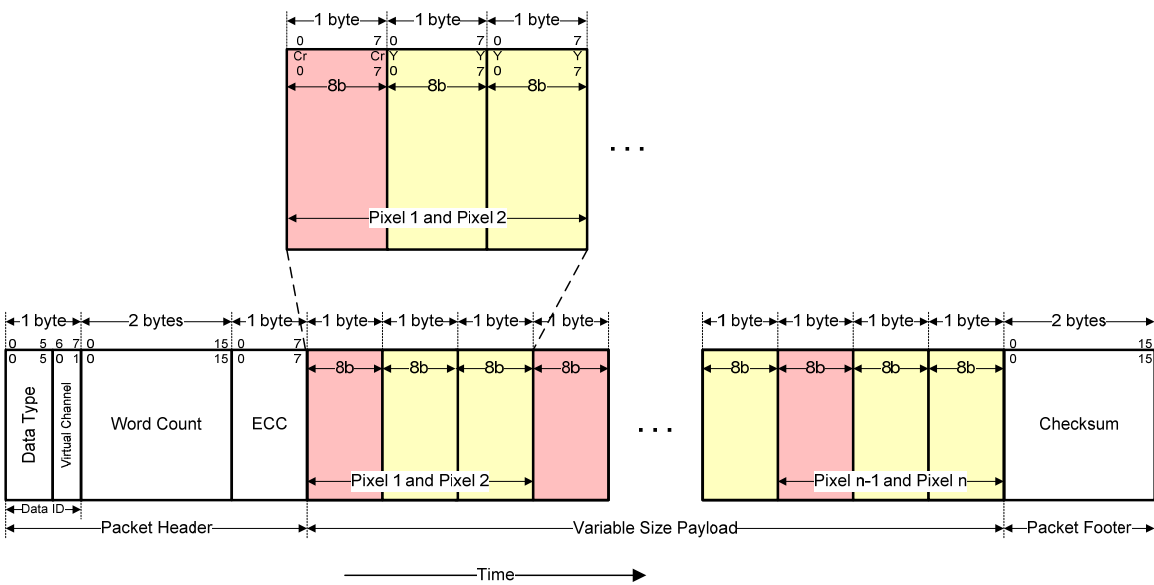
1377 A pixel shall have eight bits for each of the Y-, Cb-, and Cr-components. Within a component, the LSB is  
 1378 sent first, the MSB last. Cb- and Y-components are sent on odd lines as shown in Figure 23 while Cr- and  
 1379 Y-components are sent on even lines as shown in Figure 24.





1380  
1381

**Figure 23 12-bit per Pixel – YCbCr 4:2:0 Format (Odd Line), Long Packet**



1382  
1383  
1384

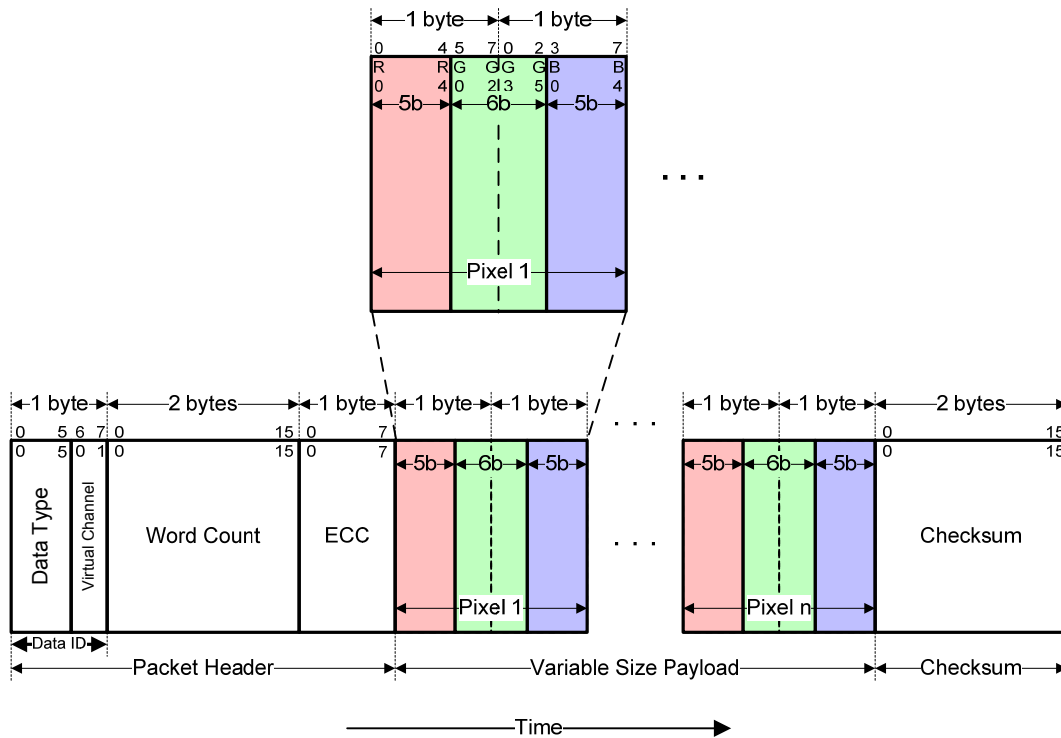
**Figure 24 12-bit per Pixel – YCbCr 4:2:0 Format (Even Line), Long Packet**

1385 The value in WC (size of payload in bytes) shall be any non-zero value divisible into an integer by three.  
1386 Allowable values for WC = {3, 6, 9,... 65 535}.

1387 **8.8.20 Packed Pixel Stream, 16-bit Format, Long Packet, Data Type 00 1110**  
1388 **(0x0E)**

1389 *Packed Pixel Stream 16-Bit Format* shown in Figure 25 is a Long packet used to transmit image data  
1390 formatted as 16-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte  
1391 WC, an ECC byte, a payload of length WC bytes and a two-byte checksum. Pixel format is five bits red, six

1392 bits green, five bits blue, in that order. Note that the “Green” component is split across two bytes. Within a  
 1393 color component, the LSB is sent first, the MSB last.



1394  
 1395

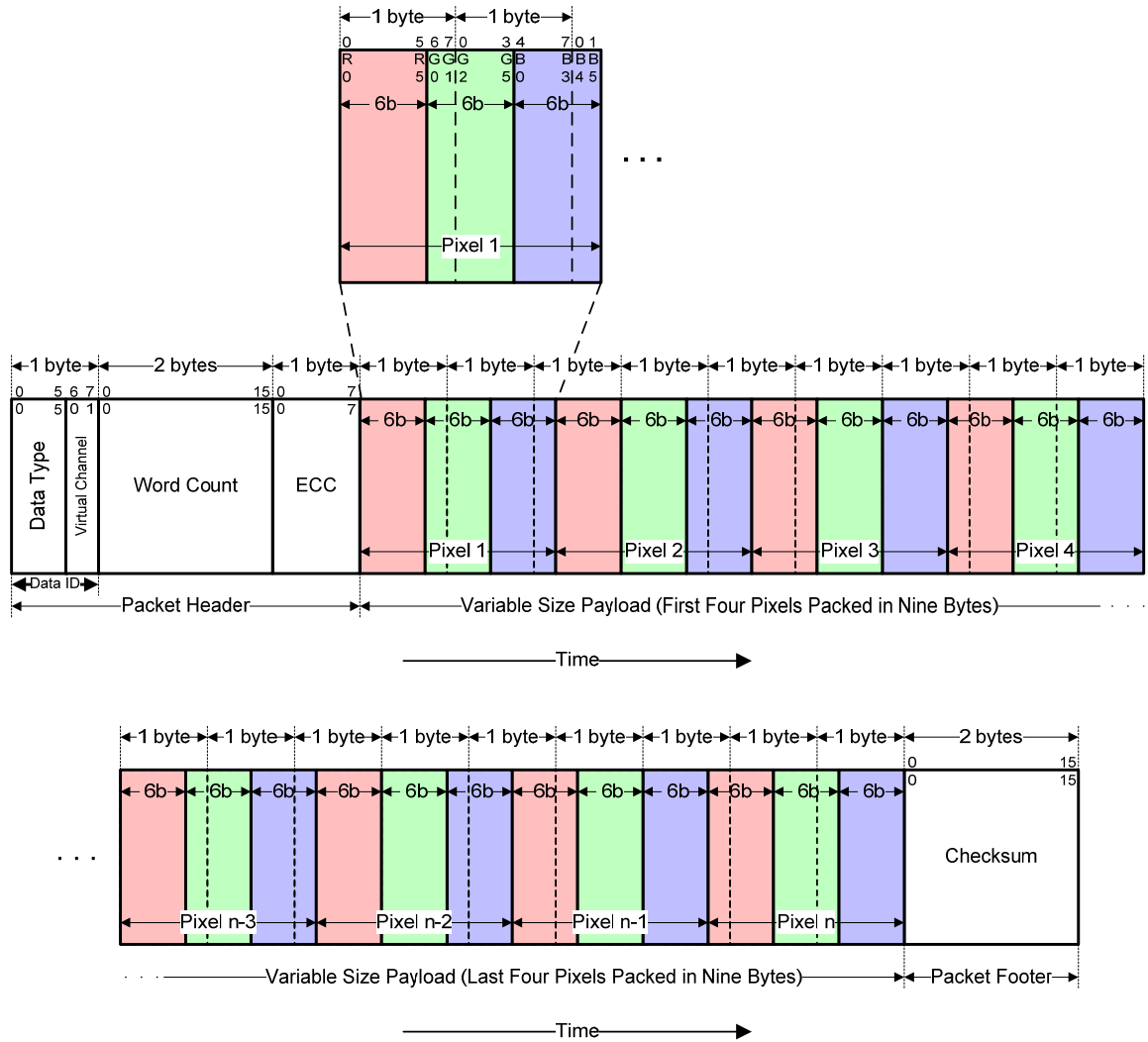
**Figure 25 16-bit per Pixel – RGB Color Format, Long Packet**

1396 With this format, pixel boundaries align with byte boundaries every two bytes. The total line width  
 1397 (displayed plus non-displayed pixels) should be a multiple of two bytes.

1398 Normally, the display module has no frame buffer of its own, so all image data shall be supplied by the host  
 1399 processor at a sufficiently high rate to avoid flicker or other visible artifacts.

1400 **8.8.21 Packed Pixel Stream, 18-bit Format, Long Packet, Data Type = 01 1110**  
 1401 **(0x1E)**

1402 *Packed Pixel Stream 18-Bit Format (Packed)* shown in Figure 26 is a Long packet. It is used to transmit  
 1403 RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet  
 1404 consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte  
 1405 Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color  
 1406 component, the LSB is sent first, the MSB last.



1407  
1408

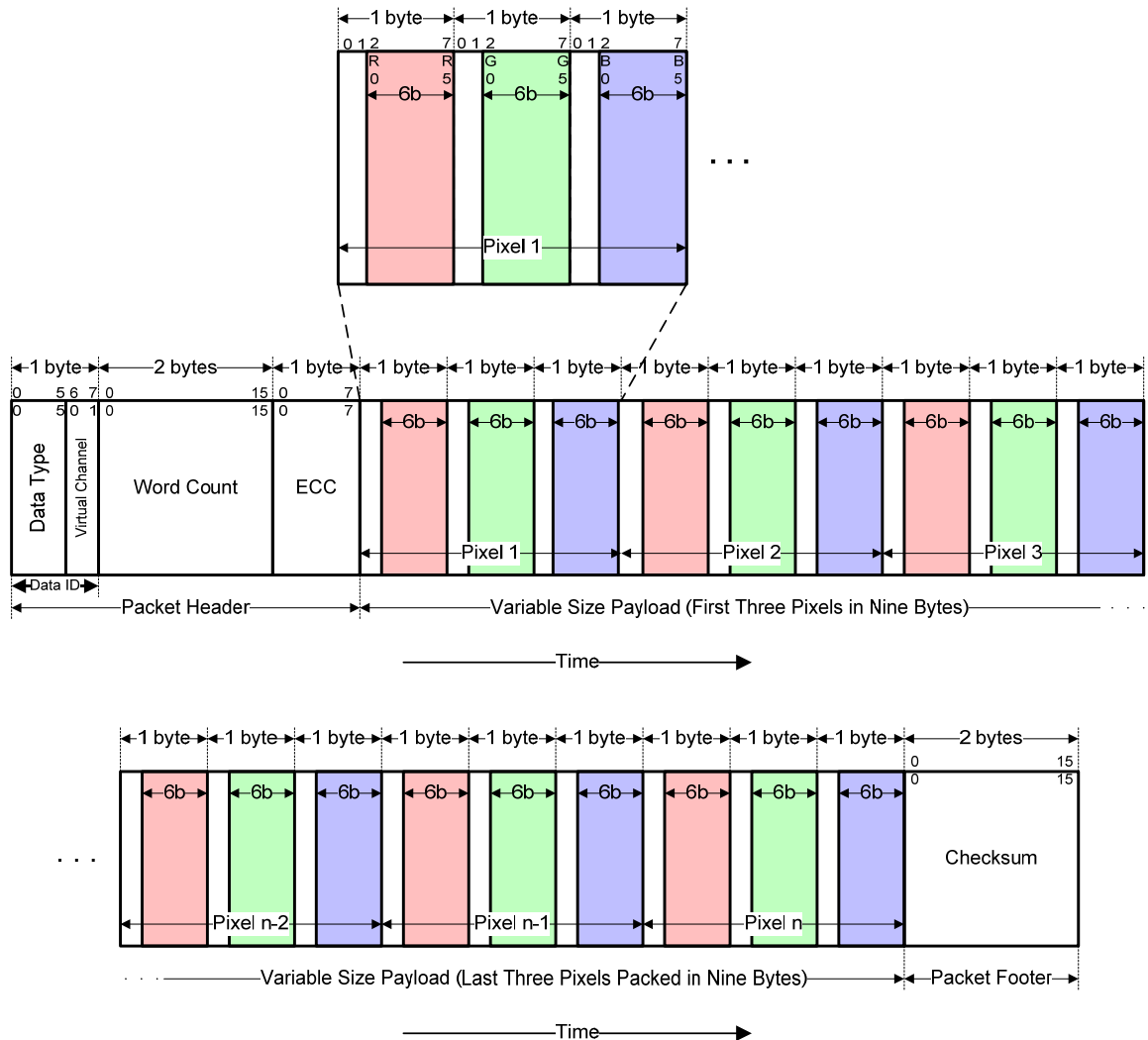
**Figure 26 18-bit per Pixel (Packed) – RGB Color Format, Long Packet**

1409 Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably,  
 1410 display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four,  
 1411 so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not  
 1412 a multiple of four pixels, the transmitter shall send additional fill pixels at the end of the display line to  
 1413 make the transmitted width a multiple of four pixels. The receiving peripheral shall not display the fill  
 1414 pixels when refreshing the display device. For example, if a display device has an active display width of  
 1415 399 pixels, the transmitter should send 400 pixels in one or more packets. The receiver should display the  
 1416 first 399 pixels and discard the last pixel of the transmission.

1417 With this format, the total line width (displayed plus non-displayed pixels) should be a multiple of four  
 1418 pixels (nine bytes).

1419 **8.8.22 Pixel Stream, 18-bit Format in Three Bytes, Long Packet, Data Type = 10**  
 1420 **1110 (0x2E)**

1421 In the *18-bit Pixel Loosely Packed* format, each R, G, or B color component is six bits, but is shifted to the  
 1422 upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte as shown in Figure 27.  
 1423 Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three  
 1424 bytes as it is transmitted across the Link. This requires more bandwidth than the “packed” format, but  
 1425 requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the  
 1426 Link.



1427

1428

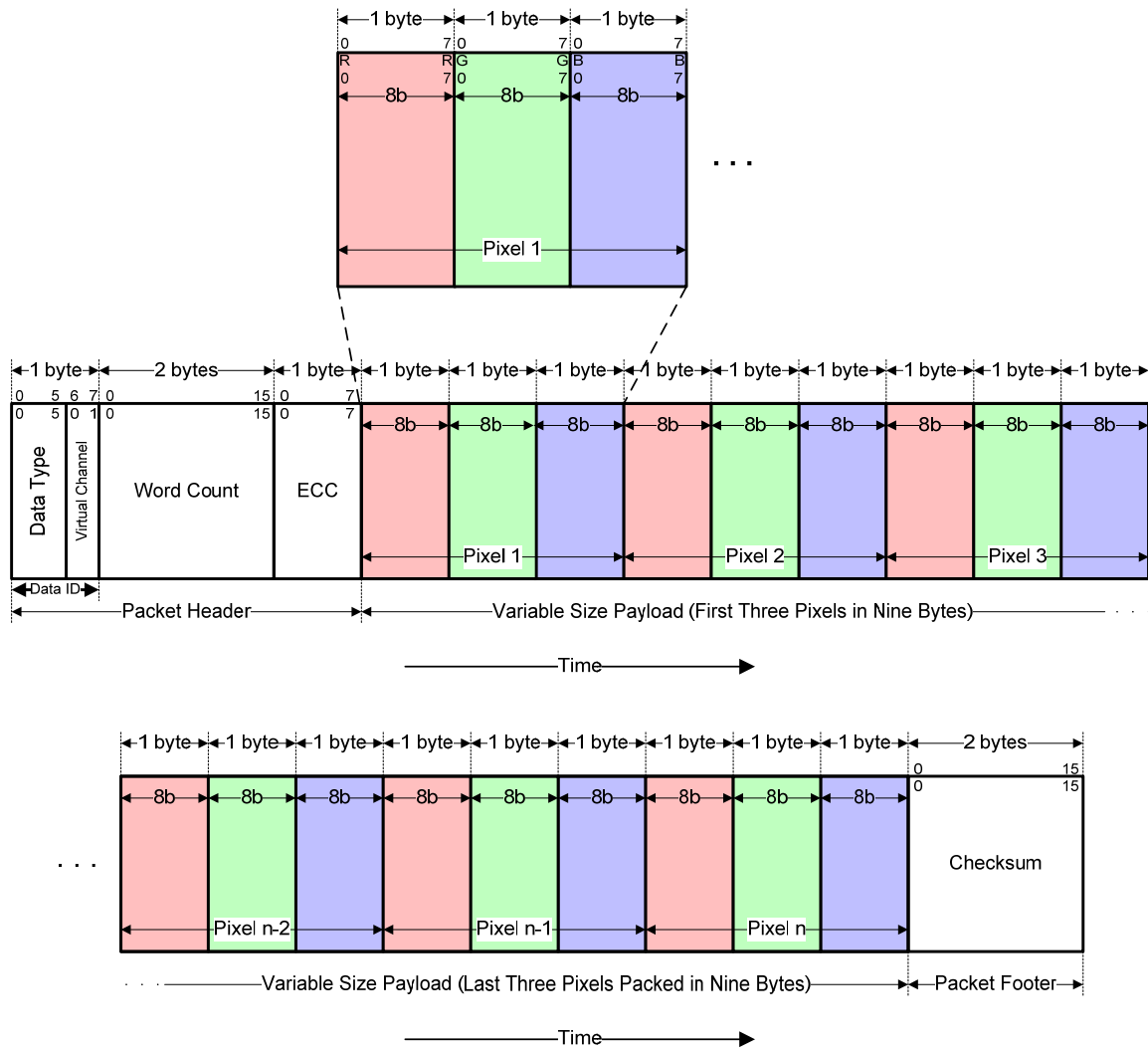
**Figure 27 18-bit per Pixel (Loosely Packed) – RGB Color Format, Long Packet**

1429 This format is used to transmit RGB image data formatted as pixels to a Video Mode display module that  
 1430 displays 18-bit pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length  
 1431 WC bytes and a two-byte Checksum. The pixel format is red (6 bits), green (6 bits) and blue (6 bits) in that  
 1432 order. Within a color component, the LSB is sent first, the MSB last.

1433 With this format, pixel boundaries align with byte boundaries every three bytes. The total line width  
 1434 (displayed plus non-displayed pixels) should be a multiple of three bytes.

1435 **8.8.23 Packed Pixel Stream, 24-bit Format, Long Packet, Data Type = 11 1110**  
 1436 **(0x3E)**

1437 *Packed Pixel Stream 24-Bit Format* shown in Figure 28 is a Long packet. It is used to transmit image data  
 1438 formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte  
 1439 WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8  
 1440 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel  
 1441 stream; no components are split across byte boundaries. Within a color component, the LSB is sent first,  
 1442 the MSB last.



1443

1444

**Figure 28 24-bit per Pixel – RGB Color Format, Long Packet**

1445 With this format, pixel boundaries align with byte boundaries every three bytes. The total line width  
 1446 (displayed plus non-displayed pixels) should be a multiple of three bytes.

## 1447 **8.8.24 DO NOT USE and Reserved Data Types**

1448 Data Type codes with four LSBs = 0000 or 1111 shall not be used. All other non-specified Data Type  
1449 codes are reserved.

1450 Note that DT encoding is specified so that all data types have at least one 0-1 or 1-0 transition in the four  
1451 bits DT bits [3:0]. This ensures a transition within the first four bits of the serial data stream of every  
1452 packet. DSI protocol or the PHY can use this information to determine quickly, following the end of each  
1453 packet, if the next bits represent the start of a new packet (transition within four bits) or an EoT sequence  
1454 (no transition for at least four bits).

## 1455 **8.9 Peripheral-to-Processor (Reverse Direction) LP Transmissions**

1456 All Command Mode systems require bidirectional capability for returning READ data, acknowledge, or  
1457 error information to the host processor. Multi-Lane systems shall use Lane 0 for all peripheral-to-processor  
1458 transmissions; other Lanes shall be unidirectional.

1459 Reverse-direction signaling shall only use LP (Low Power) mode of transmission.

1460 Simple, low-cost systems using display modules which work exclusively in Video Mode may be  
1461 configured with unidirectional DSI for all Lanes. In such systems, no acknowledge or error reporting is  
1462 possible using DSI, and no requirements specified in this section apply to such systems. However, these  
1463 systems shall have ECC checking and correction capability, which enables them to correct single-bit errors  
1464 in headers and Short packets, even if they cannot report the error.

1465 Command Mode systems that use DCS shall have a bidirectional data path. Short packets and the header of  
1466 Long packets shall use ECC and may use Checksum to provide a higher level of data integrity. The  
1467 Checksum feature enables detection of errors in the payload of Long packets.

### 1468 **8.9.1 Packet Structure for Peripheral-to-Processor LP Transmissions**

1469 Packet structure for peripheral-to-processor transactions is the same as for the processor-to-peripheral  
1470 direction.

1471 As in the processor-to-peripheral direction, two basic packet formats are specified: Short and Long. For  
1472 both types, an ECC byte shall be calculated to cover the Packet Header data. ECC calculation is the same in  
1473 the peripheral as in the host processor. For Long packets, error checking on the Data Payload, i.e. all bytes  
1474 after the Packet Header, is optional. If the Checksum is not calculated by the peripheral the Packet Footer  
1475 shall be 0x0000.

1476 BTA shall take place after every peripheral-to-processor transaction. This returns bus control to the host  
1477 processor following the completion of the LP transmission from the peripheral.

1478 Peripheral-to-processor transactions are of four basic types:

- 1479 • *Tearing Effect (TE)* is a Trigger message sent to convey display timing information to the host  
1480 processor. *Trigger* messages are single byte packets sent by a peripheral's PHY layer in response  
1481 to a signal from the DSI protocol layer. See [MIPI04] for a description of Trigger messages.
- 1482 • *Acknowledge* is a Trigger Message sent when the current transmission, as well as all preceding  
1483 transmissions since the last peripheral to host communication, i.e. either triggers or packets, is  
1484 received by the peripheral with no errors.

- 1485       • *Acknowledge and Error Report* is a Short packet sent if any errors were detected in preceding  
1486       transmissions from the host processor. Once reported, accumulated errors in the error register are  
1487       cleared.
- 1488       • *Response to Read Request* may be a Short or Long packet that returns data requested by the  
1489       preceding READ command from the processor.

## 1490   **8.9.2     System Requirements for ECC and Checksum and Packet Format**

1491   A peripheral shall implement ECC, and may optionally implement checksum.

1492   ECC support is the capability of generating ECC bytes locally from incoming packet headers and  
1493   comparing the results to the ECC fields of incoming packet headers in order to determine if an error has  
1494   occurred. DSI ECC provides detection and correction of single-bit errors and detection of multiple-bit  
1495   errors. See sections 9.4 and 9.5 for information on generating and applying ECC, respectively.

1496   For Command Mode peripherals, if a single-bit error has occurred the peripheral shall correct the error, set  
1497   the appropriate error bit (section 8.9.5) and report the error to the Host at the next available opportunity.  
1498   The packet can be used as if no error occurred. If a multiple-bit error is detected, the receiver shall drop the  
1499   packet and the rest of the transmission, set the relevant error bit and report the error back to the Host at the  
1500   next available opportunity. When the peripheral is reporting to the Host, it shall compute and send the  
1501   correct ECC based on the content of the header being transmitted.

1502   For Video Mode peripherals, if a single-bit error has occurred the peripheral shall correct the error and use  
1503   the packet as if no error occurred. If a multiple-bit error is detected, the receiver shall drop the packet and  
1504   the rest of the transmission. Since DSI Links may be unidirectional in Video Mode, error reporting  
1505   capabilities in these cases are application specific and out of scope of this document.

1506   Host processors shall implement both ECC and checksum capabilities. ECC and Checksum capabilities  
1507   shall be separately enabled or disabled so that a host processor can match a peripheral's capability when  
1508   checking return data from the peripheral. Note, in previous revisions of DSI peripheral support for ECC  
1509   was optional. See section 10.6. The mechanism for enabling and disabling Checksum capability is out of  
1510   scope for this document.

1511   An ECC byte can be applied to both Short and Long packets. Checksum bytes shall only be applied to  
1512   Long packets.

1513   Host processors and peripherals shall provide ECC support in both the Forward and Reverse  
1514   communication directions.

1515   Host processors, and peripherals that implement Checksum, shall provide Checksum capabilities in both  
1516   the Forward and Reverse communication directions.

1517   See section 8.4 for a description of the ECC and Checksum bytes.

## 1518   **8.9.3     Appropriate Responses to Commands and ACK Requests**

1519   In general, if the host processor completes a transmission to the peripheral with BTA asserted, the  
1520   peripheral shall respond with one or more appropriate packet(s), and then return bus ownership to the host  
1521   processor. If BTA is not asserted following a transmission from the host processor, the peripheral shall not  
1522   communicate an *Acknowledge* or error information back to the host processor.

1523 Interpretation of processor-to-peripheral transactions with BTA asserted, and the expected responses, are as  
1524 follows:

- 1525 • Following a non-Read command, the peripheral shall respond with *Acknowledge* if no errors were  
1526 detected and stored since the last peripheral to host communication, i.e. either triggers or packets.
- 1527 • Following a Read request, the peripheral shall send the requested READ data if no errors were  
1528 detected and stored since the last peripheral to host communication, i.e. either triggers or packets.
- 1529 • Following a Read request if only a single-bit ECC error was detected and corrected, the peripheral  
1530 shall send the requested READ data in a Long or Short packet, followed by a 4-byte *Acknowledge*  
1531 *and Error Report* packet in the same LP transmission. The Error Report shall have the *ECC Error*  
1532 *– Single Bit* flag set, as well as any error bits from any preceding transmissions stored since the  
1533 last peripheral to host communication.
- 1534 • Following a non-Read command if only a single-bit ECC error was detected and corrected, the  
1535 peripheral shall proceed to execute the command, and shall respond to BTA by sending a 4-byte  
1536 *Acknowledge and Error Report* packet. The Error Report shall have the *ECC Error – Single Bit*  
1537 flag set, as well as any error bits from any preceding transmissions stored since the last peripheral  
1538 to host communication.
- 1539 • Following a Read request, if multi-bit ECC errors were detected and not corrected, the peripheral  
1540 shall send a 4-byte *Acknowledge and Error Report* packet without sending Read data. The Error  
1541 Report shall have the *ECC Error – Multi-Bit* flag set, as well as any error bits from any preceding  
1542 transmissions stored since the last peripheral to host communication.
- 1543 • Following a non-Read command, if multi-bit ECC errors were detected and not corrected, the  
1544 peripheral shall not execute the command, and shall send a 4-byte *Acknowledge and Error Report*  
1545 packet. The Error Report shall have the *ECC Error – Multi-Bit* flag set, as well as any error bits  
1546 from any preceding transmissions stored since the last peripheral to host communication.
- 1547 • Following any command, if *SoT Error*, *SoT Sync Error* or *DSI VC ID Invalid* or DSI protocol  
1548 violation was detected, or the DSI command was not recognized, the peripheral shall send a 4-byte  
1549 *Acknowledge and Error Report* response, with the appropriate error flags set, as well as any error  
1550 bits from any preceding transmissions stored since the last peripheral to host communication, in  
1551 the two-byte error field. Only the *Acknowledge and Error Report* packet shall be transmitted; no  
1552 read or write accesses shall take place on the peripheral in response.
- 1553 • Following any command, if *EoT Sync Error* or *LP Transmit Sync Error* is detected, or a checksum  
1554 error is detected in the payload, the peripheral shall send a 4-byte *Acknowledge and Error Report*  
1555 packet with the appropriate error flags set, as well as any error bits from any preceding  
1556 transmissions stored since the last peripheral to host communication. For a read command, only  
1557 the *Acknowledge and Error Report* packet shall be transmitted; no read data shall be sent by the  
1558 peripheral in response.

1559 Refer to section 7 for how the peripheral acts when encountering Escape Mode Entry Command Error, Low  
1560 Level Transmit Sync Error and False Control Error. Section 7.2.2.2 elaborates on HS Receive Timeout  
1561 Error.

1562 Once reported to the host processor, all errors documented in this section are cleared from the Error  
1563 Register. Other error types may be detected, stored, and reported by a peripheral, but the mechanisms for  
1564 flagging, reporting, and clearing such errors are outside the scope of this document.



1565 **8.9.4 Format of Acknowledge and Error Report and Read Response Data**  
 1566 **Types**

1567 *Acknowledge and Error Report* confirms that the preceding command or data sent from the host processor  
 1568 to a peripheral was received, and indicates what types of error were detected on the transmission and any  
 1569 preceding transmissions. Note that if errors accumulate from multiple preceding transmissions, it may be  
 1570 difficult or impossible to identify which transmission contained the error. This message is a Short packet of  
 1571 four bytes, taking the form:

- 1572 • Byte 0: Data Identifier (Virtual Channel ID + Acknowledge Data Type)
- 1573 • Byte 1: Error Report bits 0-7
- 1574 • Byte 2: Error Report bits 8-15
- 1575 • ECC byte covering the header

1576 *Acknowledge* is sent using a Trigger message. See [MIPI04] for a description of Trigger messages:

- 1577 • Byte 0: 00100001 (shown here in first bit [left] to last bit [right] sequence)

1578 *Response to Read Request* returns data requested by the preceding READ command from the processor.  
 1579 These may be short or Long packets. The format for short READ packet responses is:

- 1580 • Byte 0: Data Identifier (Virtual Channel ID + Data Type)
- 1581 • Bytes 1, 2: READ data, may be one or two bytes. For single byte parameters, the parameter shall  
 1582 be returned in Byte 1 and Byte 2 shall be set to 0x00.
- 1583 • ECC byte covering the header

1584 The format for long READ packet responses is:

- 1585 • Byte 0: Data Identifier (Virtual Channel ID + Data Type)
- 1586 • Bytes 1-2: Word Count N (N = 0 to 65, 535)
- 1587 • ECC byte covering the header
- 1588 • N Bytes: READ data, may be from 1 to N bytes
- 1589 • Checksum, two bytes (16-bit checksum)
- 1590 • If Checksum is not calculated by the peripheral, send 0x0000

1591 **8.9.5 Error Reporting Format**

1592 An error report is a Short packet comprised of two bytes following the DI byte, with an ECC byte  
 1593 following the Error Report bytes. By convention, detection and reporting of each error type is signified by  
 1594 setting the corresponding bit to “1”. Table 18 shows the bit assignment for all error reporting.

1595

**Table 18 Error Report Bit Definitions**

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Peripheral Timeout Error
6	False Control Error
7	Contention Detected
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	Invalid Transmission Length
14	Reserved
15	DSI Protocol Violation

1596 The first eight bits, bit 0 through bit 7, are related to the physical layer errors that are described in sections  
 1597 7.1 and 7.2. Bits 8 and 9 are related to single-bit and multi-bit ECC errors. The remaining bits indicate DSI  
 1598 protocol-specific errors.

1599 A single-bit ECC error implies that the receiver has already corrected the error and continued with the  
 1600 previous transmission. Therefore, the data does not need to be retransmitted. A Checksum error can be  
 1601 detected and reported back to Host using a Bidirectional Link by a peripheral that has implemented CRC  
 1602 checking capability. A Host may retransmit the data or not.

1603 A DSI Data Type Not Recognized error is caused by receiving a Data Type that is either not defined or is  
 1604 defined but not implemented by the peripheral, e.g. a Command Mode peripheral may not implement  
 1605 Video Mode-specific commands such as streaming 18-bit packed RGB pixels. After encountering an  
 1606 unrecognized Data Type or multiple-bit ECC error, the receiver effectively loses packet boundaries within  
 1607 a transmission and shall drop the transmission from the point where the error was detected.

1608 DSI VC ID Invalid error is reported whenever a peripheral encounters a packet header with an  
 1609 unrecognizable VC ID.

1610 An Invalid Transmission Length error is detected whenever a peripheral receives an incorrect number of  
 1611 bytes within a particular transmission. For example, if the WC field of the header does not match the actual  
 1612 number of payload bytes for a particular packet. Depending on the number, as well as the contents, of the  
 1613 bytes following the error, there is a good chance that other types of errors such as Checksum, ECC or  
 1614 unrecognized Data Type could be detected. Another example would be a case where peripheral receives a  
 1615 short packet, i.e. four bytes plus EoT within a transmission, with a long Data Type code in the header. In  
 1616 general, the Host is responsible for maintaining the integrity of the DSI protocol. If the ECC field was  
 1617 detected correctly, implying that host may have made a mistake by inserting a wrong Data Type into the

1618 short packet, the following EoTp could be interpreted as payload for the previous packet by a peripheral.  
 1619 Depending on the WC field, a Checksum error or an unrecognized Data Type error could be detected. In  
 1620 effect, the receiver detects an invalid transmission length, sets bit 13 and reports it back to the host after the  
 1621 first BTA opportunity.

1622 In the previous example, the peripheral can also detect that an EoTp was not received correctly, which  
 1623 implies a protocol violation. Bit 15 is used to indicate DSI protocol violations where a peripheral  
 1624 encounters a situation where an expected EoTp was not received at the end of a transmission or an expected  
 1625 BTA was not received after a read request. Although host devices should maintain DSI protocol integrity,  
 1626 DSI peripherals shall be able to detect both these cases of protocol violation.

1627 Other protocol violation scenarios exist, but since there are only a limited number of bits for reporting  
 1628 errors, an extension mechanism is required. Peripheral vendors shall specify an implementation-specific  
 1629 error status register where a Host can obtain additional information regarding what type of protocol  
 1630 violation occurred by issuing a read request, e.g. via a generic DSI read packet, after receiving an  
 1631 *Acknowledge and Error Report* packet with bit 15 set. The type of protocol violations, along with the  
 1632 address of the particular error status register and the generic read packet format used to address this register  
 1633 shall be documented in the relevant peripheral data sheet. The peripheral data sheet and documentation  
 1634 format is out of scope for this document.

## 1635 8.10 Peripheral-to-Processor Transactions – Detailed Format Description

1636 Table 19 presents the complete set of peripheral-to-processor Data Types.

1637 **Table 19 Data Types for Peripheral-sourced Packets**

Data Type, hex	Data Type, binary	Description	Packet Size
0x00 – 0x01	00 000X	Reserved	Short
0x02	00 0010	Acknowledge and Error Report	Short
0x03 – 0x07	00 0011 – 00 0111	Reserved	
0x08	00 1000	End of Transmission packet (EoTp)	Short
0x09 – 0x10	00 1001 – 01 0000	Reserved	
0x11	01 0001	Generic Short READ Response, 1 byte returned	Short
0x12	01 0010	Generic Short READ Response, 2 bytes returned	Short
0x13 – 0x19	01 0011 – 01 1001	Reserved	
0x1A	01 1010	Generic Long READ Response	Long
0x1B	01 1011	Reserved	
0x1C	01 1100	DCS Long READ Response	Long
0x1D – 0x20	01 1101 – 10 0000	Reserved	
0x21	10 0001	DCS Short READ Response, 1 byte returned	Short
0x22	10 0010	DCS Short READ Response, 2 bytes returned	Short
0x23 – 0x3F	10 0011 –	Reserved	

Data Type, hex	Data Type, binary	Description	Packet Size
	11 1111		

1638 **8.10.1 Acknowledge and Error Report, Data Type 00 0010 (0x02)**

1639 *Acknowledge and Error Report* is sent in response to any command, or read request, with BTA asserted  
 1640 when a reportable error is detected in the preceding, or earlier, transmission from the host processor. In the  
 1641 case of a correctable ECC error, this packet is sent following the requested READ data packet in the same  
 1642 LP transmission.

1643 When multiple peripherals share a single DSI, the *Acknowledge and Error Report* packet shall be tagged  
 1644 with the Virtual Channel ID 0b00.

1645 Although some errors, such as a correctable ECC error, can be associated with a packet targeted at a  
 1646 specific peripheral, an uncorrectable error cannot be associated with any particular peripheral. Additionally,  
 1647 many detectable error types are PHY-level transmission errors and cannot be associated with specific  
 1648 packets.

1649 **8.10.2 Generic Short Read Response, 1 or 2 Bytes, Data Types = 01 0001 or 01**  
 1650 **0010, Respectively**

1651 This is the short-packet response to *Generic READ Request*. Packet composition is the Data Identifier (DI)  
 1652 byte, two bytes of payload data and an ECC byte. The number of valid bytes is indicated by the Data Type  
 1653 LSBs, DT bits [1:0]. DT = 01 0001 indicates one byte and DT = 01 0010 indicates two bytes are returned.  
 1654 For a single-byte read response, valid data shall be returned in the first (LS) byte, and the second (MS) byte  
 1655 shall be sent as 0x00.

1656 This form of data transfer may be used for other features incorporated on the peripheral, such as a touch-  
 1657 screen integrated on the display module. Data formats for such applications are outside the scope of this  
 1658 document.

1659 If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the  
 1660 requested READ data packet shall not be sent and only the *Acknowledge and Error Report* packet shall be  
 1661 sent.

1662 **8.10.3 Generic Long Read Response with Optional Checksum, Data Type = 01**  
 1663 **1010 (0x1A)**

1664 This is the long-packet response to *Generic READ Request*. Packet composition is the Data Identifier (DI)  
 1665 byte followed by a two-byte Word Count, an ECC byte, N bytes of payload, and a two-byte Checksum. If  
 1666 the peripheral is Checksum capable, it shall return a calculated two-byte Checksum appended to the N-byte  
 1667 payload data. If the peripheral does not support Checksum it shall return 0x0000.

1668 If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the  
 1669 requested READ data packet shall not be sent and only the *Acknowledge and Error Report* packet shall be  
 1670 sent.

1671 **8.10.4 DCS Long Read Response with Optional Checksum, Data Type 01 1100**  
 1672 **(0x1C)**

1673 This is a Long packet response to *DCS Read Request*. Packet composition is the Data Identifier (DI) byte  
 1674 followed by a two-byte Word Count, an ECC byte, N bytes of payload, and a two-byte Checksum. If the  
 1675 peripheral is Checksum capable, it shall return a calculated two-byte Checksum appended to the N-byte  
 1676 payload data. If the peripheral does not support Checksum it shall return 0x0000.

1677 If the DCS command itself is possibly corrupt, due to uncorrectable ECC error, SoT or SoT Sync error, the  
 1678 requested READ data packet shall not be sent and only the *Acknowledge and Error Report* packet shall be  
 1679 sent.

1680 **8.10.5 DCS Short Read Response, 1 or 2 Bytes, Data Types = 10 0001 or 10**  
 1681 **0010, Respectively**

1682 This is the short-packet response to *DCS Read Request*. Packet composition is the Data Identifier (DI) byte,  
 1683 two bytes of payload data and an ECC byte. The number of valid bytes is indicated by the Data Type LSBs,  
 1684 DT bits [1:0]. DT = 01 0001 indicates one byte and DT = 01 0010 indicates two bytes are returned. For a  
 1685 single-byte read response, valid data shall be returned in the first (LS) byte, and the second (MS) byte shall  
 1686 be sent as 0x00.

1687 If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the  
 1688 requested READ data packet shall not be sent and only the *Acknowledge and Error Report* packet shall be  
 1689 sent.

1690 **8.10.6 Multiple Transmissions and Error Reporting**

1691 A peripheral shall report all errors documented in Table 18, when a command or request is followed by  
 1692 BTA giving bus possession to the peripheral. Peripheral shall accumulate errors from multiple transactions  
 1693 up until a time that host is issuing a BTA. After that, only one ACK Trigger Message or *Acknowledge and*  
 1694 *Error Report* packet shall be returned regardless of the number of packets or transmissions. Notice that host  
 1695 may not be able to associate each error to a particular packet or transmission causing that error.

1696 If receiving an *Acknowledge and Error Report* for each and every packet is desired, software can send  
 1697 individual packets within separate transmissions. In this case, a BTA follows each individual transmission.  
 1698 Furthermore, the peripheral may choose to store other information about errors that may be recovered by  
 1699 the host processor at a later time. The format and access mechanism of such additional error information is  
 1700 outside the scope of this document.

1701 **8.10.7 Clearing Error Bits**

1702 Errors shall be accumulated by the peripheral during single or multiple transmissions and only cleared after  
 1703 they have been reported back to the host processor. Errors are transmitted as part of an *Acknowledge and*  
 1704 *Error Report* response after the host issues a BTA.

1705 **8.11 Video Mode Interface Timing**

1706 Video Mode peripherals require pixel data delivered in real time. This section specifies the format and  
 1707 timing of DSI traffic for this type of display module.

### 1708 8.11.1 Transmission Packet Sequences

1709 DSI supports several formats, or packet sequences, for Video Mode data transmission. The peripheral's  
 1710 timing requirements dictate which format is appropriate. In the following sections, *Burst Mode* refers to  
 1711 time-compression of the RGB pixel (active video) portion of the transmission. In addition, these terms are  
 1712 used throughout the following sections:

- 1713 • Non-Burst Mode with Sync Pulses – enables the peripheral to accurately reconstruct original video  
 1714 timing, including sync pulse widths.
- 1715 • Non-Burst Mode with Sync Events – similar to above, but accurate reconstruction of sync pulse  
 1716 widths is not required, so a single *Sync Event* is substituted.
- 1717 • Burst mode – RGB pixel packets are time-compressed, leaving more time during a scan line for  
 1718 LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

1719 Note that for accurate reconstruction of timing, packet overhead including Data ID, ECC, and Checksum  
 1720 bytes should be taken into consideration.

1721 The host processor shall support all of the packet sequences in this section. A Video Mode peripheral shall  
 1722 support at least one of the packet sequences in this section. The peripheral shall not require any additional  
 1723 constraints regarding packet sequence or packet timing. The peripheral supplier shall document all relevant  
 1724 timing parameters listed in Table 20.

1725 In the following figures the Blanking or Low-Power Interval (BLLP) is defined as a period during which  
 1726 video packets such as pixel-stream and sync event packets are not actively transmitted to the peripheral.

1727 To enable PHY synchronization the host processor should periodically end HS transmission and drive the  
 1728 Data Lanes to the LP state. This transition should take place at least once per frame; shown as LPM in the  
 1729 figures in this section. It is recommended to return to LP state once per scanline during the horizontal  
 1730 blanking time. Regardless of the frequency of BLLP periods, the host processor is responsible for meeting  
 1731 all documented peripheral timing requirements. Note, at lower frequencies BLLP periods will approach, or  
 1732 become, zero, and burst mode will be indistinguishable from non-burst mode.

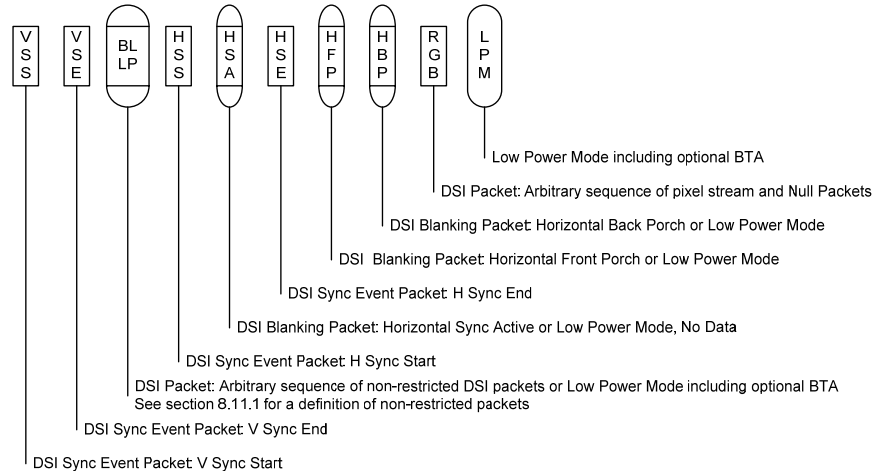
1733 During the BLLP the DSI Link may do any of the following:

- 1734 • Remain in Idle Mode with the host processor in LP-11 state and the peripheral in LP-RX
- 1735 • Transmit one or more non-video packets from the host processor to the peripheral using Escape  
 1736 Mode
- 1737 • Transmit one or more non-video packets from the host processor to the peripheral using HS Mode
- 1738 • If the previous processor-to-peripheral transmission ended with BTA, transmit one or more  
 1739 packets from the peripheral to the host processor using Escape Mode
- 1740 • Transmit one or more packets from the host processor to a different peripheral using a different  
 1741 Virtual Channel ID

1742 The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host  
 1743 processor may compose any sequence of packets, including iterations, within the limits of the packet format  
 1744 definitions. For all timing cases, the first line of a frame shall start with VSS; all other lines shall start with  
 1745 VSE or HSS. Note that the position of synchronization packets, such as VSS and HSS, in time is of utmost  
 1746 importance since this has a direct impact on the visual performance of the display panel.

1747 Normally, RGB pixel data is sent with one full scanline of pixels in a single packet. If necessary, a  
 1748 horizontal scanline of active pixels may be divided into two or more packets. However, individual pixels  
 1749 shall not be split across packets.

1750 Transmission packet components used in the figures in this section are defined in Figure 29 unless  
 1751 otherwise specified.



1752

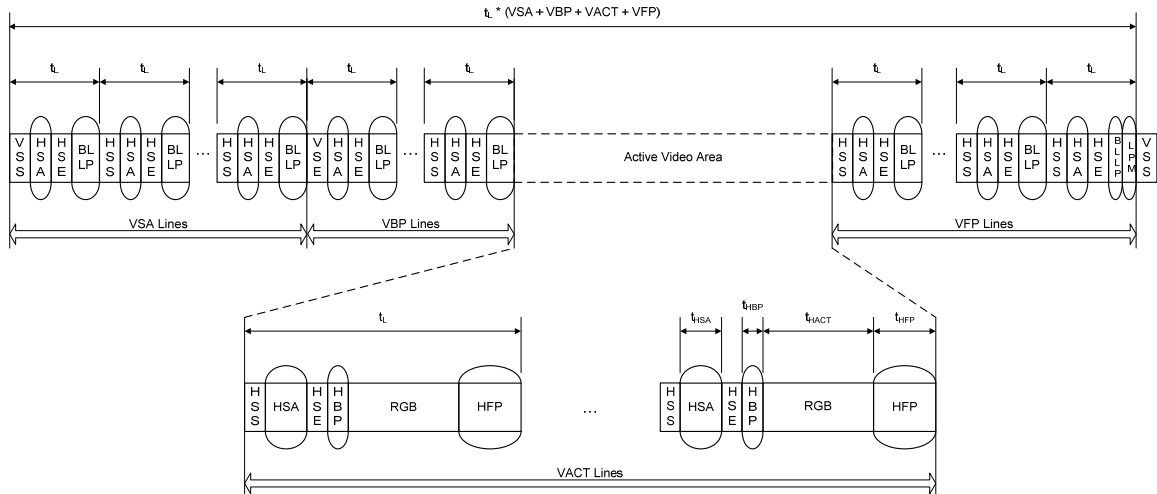
1753

**Figure 29 Video Mode Interface Timing Legend**

1754 If a peripheral timing specification for HBP or HFP minimum period is zero, the corresponding Blanking  
 1755 Packet may be omitted. If the HBP or HFP maximum period is zero, the corresponding blanking packet  
 1756 shall be omitted.

### 1757 **8.11.2 Non-Burst Mode with Sync Pulses**

1758 With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes  
 1759 matching DPI pixel-transmission rates, and widths of timing events like sync pulses. Accordingly,  
 1760 synchronization periods are defined using packets transmitting both start and end of sync pulses. An  
 1761 example of this mode is shown in Figure 30.



1762  
1763

1764 **Figure 30 Video Mode Interface Timing: Non-Burst Transmission with Sync Start and End**

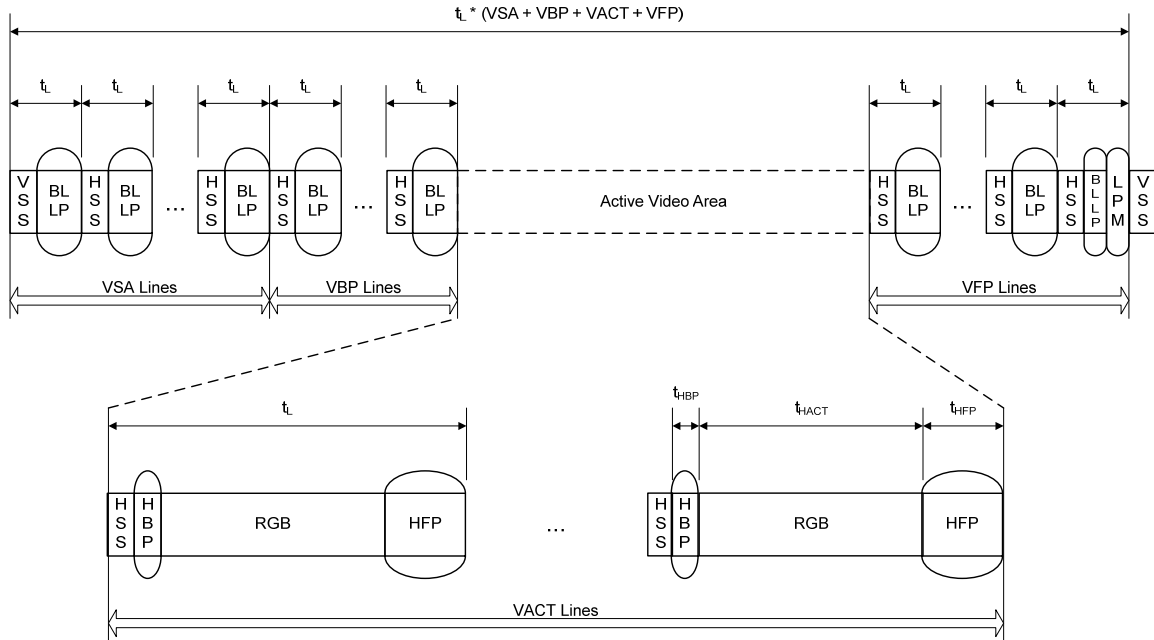
1765 Normally, periods shown as HSA (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP  
1766 (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead)  
1767 calculated to match the period specified by the peripheral's data sheet. Alternatively, if there is sufficient  
1768 time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a  
1769 Blanking Packet, thus saving power. During HSA, HBP and HFP periods, the bus should stay in the LP-11  
1770 state.

1771 Refer to Annex C for the method of Video Mode interface timing for non-burst transmission with Sync  
1772 Start and Sync End sourcing interlaced video.

### 1773 8.11.3 Non-Burst Mode with Sync Events

1774 This mode is a simplification of the format described in section 8.11.2. Only the start of each  
1775 synchronization pulse is transmitted. The peripheral may regenerate sync pulses as needed from each Sync  
1776 Event packet received. Pixels are transmitted at the same rate as they would in a corresponding parallel  
1777 display interface such as DPI-2. An example of this mode is shown in Figure 31.





1778  
1779

1780 **Figure 31 Video Mode Interface Timing: Non-burst Transmission with Sync Events**

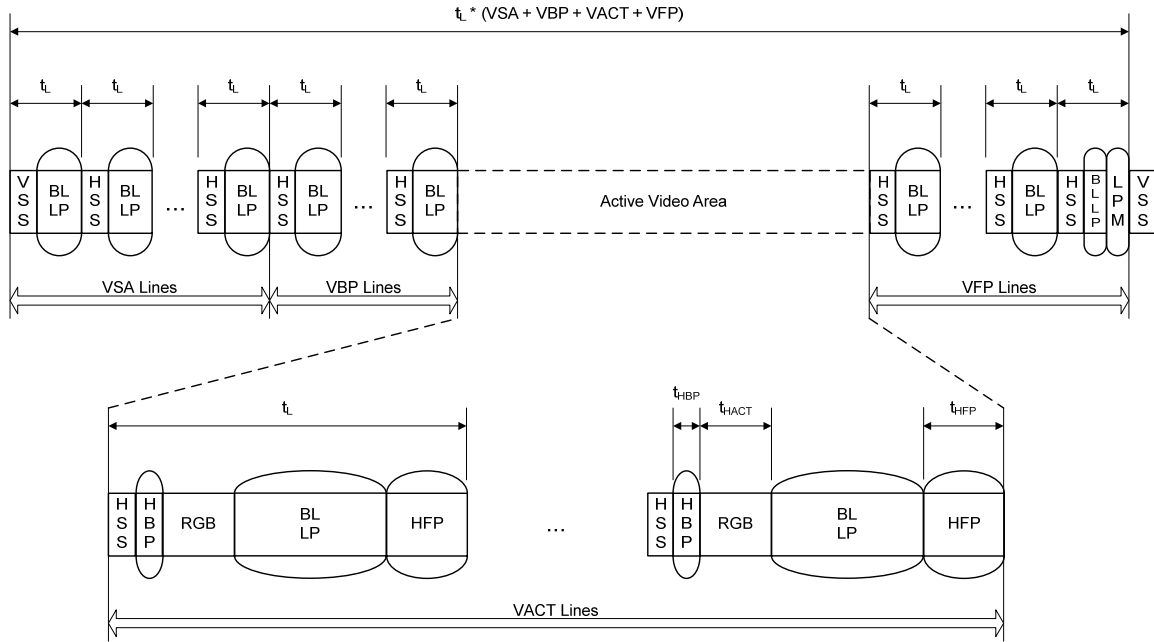
1781 As with the previous Non-Burst Mode, if there is sufficient time to transition from HS to LP mode and  
1782 back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

1783 Refer to Annex C for the method of Video Mode interface timing for non-burst transmission with Sync  
1784 Events sourcing interlaced video.

#### 1785 **8.11.4 Burst Mode**

1786 In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format.  
1787 This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time  
1788 for other data transmissions over the Link in either direction.

1789 There may be a line buffer or similar memory on the peripheral to accommodate incoming data at high  
1790 speed. Following HS pixel data transmission, the bus may stay in HS Mode for sending blanking packets or  
1791 go to Low Power Mode, during which it may remain idle, i.e. the host processor remains in LP-11 state, or  
1792 LP transmission may take place in either direction. If the peripheral takes control of the bus for sending  
1793 data to the host processor, its transmission time shall be limited to ensure data underflow does not occur  
1794 from its internal buffer memory to the display device. An example of this mode is shown in Figure 32.



1795  
1796

1797

**Figure 32 Video Mode Interface Timing: Burst Transmission**

1798 Similar to the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and  
1799 back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

1800 **8.11.5 Parameters**

1801 Table 20 documents the parameters used in the preceding figures. Peripheral supplier companies are  
1802 responsible for specifying suitable values for all blank fields in the table. The host processor shall meet  
1803 these requirements to ensure interoperability.

1804 For periods when Data Lanes are in LP Mode, the peripheral shall also specify whether the DSI Clock Lane  
1805 may go to LP. The host processor is responsible for meeting minimum timing relationships between clock  
1806 activity and HS transmission on the Data Lanes as documented in [MIPI04].

1807

**Table 20 Required Peripheral Timing Parameters**

Parameter	Description	Minimum	Maximum	Units	Comment
$b_{r_{PHY}}$	Bit rate total on all Lanes			Mbps	Depends on PHY implementation
$t_L$	Line time			$\mu s$	Define range to meet frame rate
$t_{HSA}$	Horizontal sync active			$\mu s$	
$t_{HBP}$	Horizontal back porch			$\mu s$	
$t_{HACT}$	Time for image data			$\mu s$	Defining min = 0 allows max PHY speed
HACT	Active pixels per line			pixels	

Parameter	Description	Minimum	Maximum	Units	Comment
t <sub>HFP</sub>	Horizontal front porch			μs	No upper limit as long as line time is met
VSA	Vertical sync active			lines	Number of lines in the vertical sync area
VBP	Vertical back porch			lines	
VACT	Active lines per frame			lines	
VFP	Vertical front porch			lines	

## 1808 8.12 TE Signaling in DSI

1809 A Command Mode display module has its own timing controller and local frame buffer for display refresh.  
 1810 In some cases the host processor needs to be notified of timing events on the display module, e.g. the start  
 1811 of vertical blanking or similar timing information. In a traditional parallel-bus interface like DBI-2, a  
 1812 dedicated signal wire labeled TE (Tearing Effect) is provided to convey such timing information to the host  
 1813 processor. In a DSI system, the same information, with reasonably low latency, shall be transmitted from  
 1814 the display module to the host processor when requested, using the bidirectional Data Lane.

1815 The PHY for DSI has no inherent interrupt capability from peripheral to host processor so the host  
 1816 processor shall either rely on polling, or it shall give bus ownership to the peripheral for extended periods,  
 1817 as it does not know when the peripheral will send the TE message.

1818 For polling to the display module, the host processor shall detect the current scan line information with a  
 1819 DCS command such as get\_scan\_line to avoid Tearing Effects. For TE-reporting from the display module,  
 1820 the TE-reporting function is enabled and disabled by three DCS commands to the display module's  
 1821 controller: set\_tear\_on, set\_tear\_scanline, and set\_tear\_off. See [MIPI01] for details.

1822 set\_tear\_on and set\_tear\_scanline are sent to the display module as DSI Data Type 0x15 (DCS Short Write,  
 1823 one parameter) and DSI Data Type 0x39 (DCS Long Write/write\_LUT), respectively. The host processor  
 1824 ends the transmission with Bus Turn-Around asserted, giving bus possession to the display module. Since  
 1825 the display module's DSI Protocol layer does not interpret DCS commands, but only passes them through  
 1826 to the display controller, it responds with a normal Acknowledge and returns bus possession to the host  
 1827 processor. In this state, the display module cannot report TE events to the host processor since it does not  
 1828 have bus possession.

1829 To enable TE-reporting, the host processor shall give bus possession to the display module without an  
 1830 accompanying DSI command transmission after TE reporting has been enabled. This is accomplished by  
 1831 the host processor's protocol logic asserting (internal) Bus Turn-Around signal to its D-PHY functional  
 1832 block. The PHY layer will then initiate a Bus Turn-Around sequence in LP mode, which gives bus  
 1833 possession to the display module.

1834 Since the timing of a TE event is, by definition, unknown to the host processor, the host processor shall  
 1835 give bus possession to the display module and then wait for up to one video frame period for the TE  
 1836 response. During this time, the host processor cannot send new commands, or requests to the display  
 1837 module, because it does not have bus possession.

1838 When the TE event takes place the display module shall send TE event information in LP mode using a  
 1839 specified trigger message available with D-PHY protocol via the following sequence:

- 1840 • The display module shall send the LP Escape Mode sequence

1841           • The display module shall then send the trigger message byte 01011101 (shown here in first bit to  
1842           last bit sequence)

1843           • The display module shall then return bus possession to the host processor

1844       This Trigger Message is reserved by DSI for TE signaling only and shall not be used for any other purpose  
1845       in a DSI-compliant interface.

1846       See [MIPI01] for detailed descriptions of the TE related commands, and command and parameter formats.  
1847

## 1848 **9 Error-Correcting Code (ECC) and Checksum**

### 1849 **9.1 Packet Header Error Detection/Correction**

1850 The host processor in a DSI-based system shall generate an error-correction code (ECC) and append it to  
 1851 the header of every packet sent to the peripheral. The ECC takes the form of a single byte following the  
 1852 header bytes. The ECC byte shall provide single-bit error correction and 2-bit error detection for the entire  
 1853 Packet Header. See Figure 13 and Figure 14 for descriptions of the Long and Short Packet Headers,  
 1854 respectively.

1855 ECC shall always be generated and appended in the Packet Header from the host processor. Peripherals  
 1856 with Bidirectional Links shall also generate and send ECC.

1857 Peripherals in unidirectional DSI systems, although they cannot report errors to the host, shall still take  
 1858 advantage of ECC for correcting single-bit errors in the Packet Header.

### 1859 **9.2 Hamming Code Theory**

1860 The number of parity or error check bits required is given by the Hamming rule, and is a function of the  
 1861 number of bits of information transmitted. The Hamming rule is expressed by the following inequality:

1862 
$$d + p + 1 <= 2^p$$
 where  $d$  is the number of data bits and  $p$  is the number of parity bits.

1863 The result of appending the computed parity bits to the data bits is called the Hamming code word. The size  
 1864 of the code word  $c$  is  $d+p$ , and a Hamming code word is described by the ordered set  $(c, d)$ .

1865 A Hamming code word is generated by multiplying the data bits by a generator matrix  $\mathbf{G}$ . This  
 1866 multiplication's result is called the code word vector  $(c1, c2, c3, \dots, cn)$ , consisting of the original data bits  
 1867 and the calculated parity bits. The generator matrix  $\mathbf{G}$  used in constructing Hamming codes consists of  $\mathbf{I}$ ,  
 1868 the identity matrix, and a parity generation matrix  $\mathbf{A}$ :

1869 
$$\mathbf{G} = [ \mathbf{I} \mid \mathbf{A} ]$$

1870 The Packet Header plus the ECC code can be obtained as:  $\text{PH} = \text{p} * \mathbf{G}$  where  $\text{p}$  represents the header and  $\mathbf{G}$  is  
 1871 the corresponding generator matrix.

1872 Validating the received code word  $r$  involves multiplying it by a parity check to form  $s$ , the syndrome or  
 1873 parity check vector:  $s = \mathbf{H} * \text{PH}$  where  $\text{PH}$  is the received Packet Header and  $\mathbf{H}$  is the parity check matrix:

1874 
$$\mathbf{H} = [ \mathbf{A}^T \mid \mathbf{I} ]$$

1875 If all elements of  $s$  are zero, the code word was received correctly. If  $s$  contains non-zero elements, then at  
 1876 least one error is present. If the header has a single-bit error, then the syndrome  $s$  matches one of the  
 1877 elements of  $\mathbf{H}$ , which will point to the bit in error. Furthermore, if the bit in error is a parity bit, then the  
 1878 syndrome will be one of the elements on  $\mathbf{I}$ , or else it will be the data bit identified by the position of the  
 1879 syndrome in  $\mathbf{A}^T$ .

### 1880 9.3 Hamming-modified Code Applied to DSI Packet Headers

1881 Hamming codes use parity to correct a single-bit error or detect a two-bit error, but are not capable of doing  
 1882 both simultaneously. DSI uses Hamming-modified codes where an extra parity bit is used to support both  
 1883 single error correction as well as two-bit error detection. For example a 7+1 bit Hamming-modified code  
 1884 (72, 64) allows for protection of up to 64 data bits. DSI systems shall use a 5+1 bit Hamming-modified  
 1885 code (30, 24), allowing for protection of up to twenty-four data bits. The addition of a parity bit allows a  
 1886 five bit Hamming code to correct a single-bit error and detect a two-bit error simultaneously.

1887 Since Packet Headers are fixed at four bytes (twenty-four data bits and eight ECC bits), P6 and P7 of the  
 1888 ECC byte are unused and shall be set to zero by the transmitter. The receiver shall ignore P6 and P7 and set  
 1889 both bits to zero before processing ECC. Table 21 shows a compact way to specify the encoding of parity  
 1890 and decoding of syndromes.

1891 **Table 21 ECC Syndrome Association Matrix**

	d2d1d0							
d5d4d3	0b000	0b001	0b010	0b011	0b100	0b101	0b110	0b111
0b000	0x07	0x0B	0x0D	0x0E	0x13	0x15	0x16	0x19
0b001	0x1A	0x1C	0x23	0x25	0x26	0x29	0x2A	0x2C
0b010	0x31	0x32	0x34	0x38	0x1F	0x2F	0x37	0x3B
0b011	0x43	0x45	0x46	0x49	0x4A	0x4C	0x51	0x52
0b100	0x54	0x58	0x61	0x62	0x64	0x68	0x70	0x83
0b101	0x85	0x86	0x89	0x8A	0x3D	0x3E	0x4F	0x57
0b110	0x8C	0x91	0x92	0x94	0x98	0xA1	0xA2	0xA4
0b111	0xA8	0xB0	0xC1	0xC2	0xC4	0xC8	0xD0	0xE0

1892 Each cell in the matrix represents a syndrome and each syndrome in the matrix is MSB left aligned:

1893 e.g. 0x07=0b0000\_0111=P7P6P5P4P3P2P1P0

1894 The top row defines the three LSB of data position bit, and the left column defines the three MSB of data  
 1895 position bit for a total of 64-bit positions.

1896 e.g. 38th bit position (D37) is encoded 0b100\_101 and has the syndrome 0x68.

1897 To correct a single bit error, the syndrome shall be one of the syndromes in the table, which will identify  
 1898 the bit position in error. The syndrome is calculated as:

1899  $S = P_{SEND} \wedge P_{RECEIVED}$  where  $P_{SEND}$  is the 6-bit ECC field in the header and  $P_{RECEIVED}$  is the  
 1900 calculated parity of the received header.

1901 Table 22 represents the same information as in Table 21, organized to provide better insight into how parity  
 1902 bits are formed from data bits.

1903

**Table 22 ECC Parity Generation Rules**

Data Bit	P7	P6	P5	P4	P3	P2	P1	P0	Hex
0	0	0	0	0	0	1	1	1	0x07
1	0	0	0	0	1	0	1	1	0x0B
2	0	0	0	0	1	1	0	1	0x0D
3	0	0	0	0	1	1	1	0	0x0E
4	0	0	0	1	0	0	1	1	0x13
5	0	0	0	1	0	1	0	1	0x15
6	0	0	0	1	0	1	1	0	0x16
7	0	0	0	1	1	0	0	1	0x19
8	0	0	0	1	1	0	1	0	0x1A
9	0	0	0	1	1	1	0	0	0x1C
10	0	0	1	0	0	0	1	1	0x23
11	0	0	1	0	0	1	0	1	0x25
12	0	0	1	0	0	1	1	0	0x26
13	0	0	1	0	1	0	0	1	0x29
14	0	0	1	0	1	0	1	0	0x2A
15	0	0	1	0	1	1	0	0	0x2C
16	0	0	1	1	0	0	0	1	0x31
17	0	0	1	1	0	0	1	0	0x32
18	0	0	1	1	0	1	0	0	0x34
19	0	0	1	1	1	0	0	0	0x38
20	0	0	0	1	1	1	1	1	0x1F
21	0	0	1	0	1	1	1	1	0x2F
22	0	0	1	1	0	1	1	1	0x37
23	0	0	1	1	1	0	1	1	0x3B
24	0	1	0	0	0	0	1	1	0x43
25	0	1	0	0	0	1	0	1	0x45
26	0	1	0	0	0	1	1	0	0x46
27	0	1	0	0	1	0	0	1	0x49
28	0	1	0	0	1	0	1	0	0x4A
29	0	1	0	0	1	1	0	0	0x4C
30	0	1	0	1	0	0	0	1	0x51
31	0	1	0	1	0	0	1	0	0x52
32	0	1	0	1	0	1	0	0	0x54
33	0	1	0	1	1	0	0	0	0x58

Data Bit	P7	P6	P5	P4	P3	P2	P1	P0	Hex
34	0	1	1	0	0	0	0	1	0x61
35	0	1	1	0	0	0	1	0	0x62
36	0	1	1	0	0	1	0	0	0x64
37	0	1	1	0	1	0	0	0	0x68
38	0	1	1	1	0	0	0	0	0x70
39	1	0	0	0	0	0	1	1	0x83
40	1	0	0	0	0	1	0	1	0x85
41	1	0	0	0	0	1	1	0	0x86
42	1	0	0	0	1	0	0	1	0x89
43	1	0	0	0	1	0	1	0	0x8A
44	0	0	1	1	1	1	0	1	0x3D
45	0	0	1	1	1	1	1	0	0x3E
46	0	1	0	0	1	1	1	1	0x4F
47	0	1	0	1	0	1	1	1	0x57
48	1	0	0	0	1	1	0	0	0x8C
49	1	0	0	1	0	0	0	1	0x91
50	1	0	0	1	0	0	1	0	0x92
51	1	0	0	1	0	1	0	0	0x94
52	1	0	0	1	1	0	0	0	0x98
53	1	0	1	0	0	0	0	1	0xA1
54	1	0	1	0	0	0	1	0	0xA2
55	1	0	1	0	0	1	0	0	0xA4
56	1	0	1	0	1	0	0	0	0xA8
57	1	0	1	1	0	0	0	0	0xB0
58	1	1	0	0	0	0	0	1	0xC1
59	1	1	0	0	0	0	1	0	0xC2
60	1	1	0	0	0	1	0	0	0xC4
61	1	1	0	0	1	0	0	0	0xC8
62	1	1	0	1	0	0	0	0	0xD0
63	1	1	1	0	0	0	0	0	0xE0

1904 To derive parity bit P3, the “ones” in the P3 column define if the corresponding bit position Di (as noted in  
 1905 the green column) is used in calculation of P3 parity bit or not. For example,

1906 
$$P3 = D1 \wedge D2 \wedge D3 \wedge D7 \wedge D8 \wedge D9 \wedge D13 \wedge D14 \wedge D15 \wedge D19 \wedge D20 \wedge D21 \wedge D23$$



1907 The first twenty-four data bits, D0 to D23, in Table 22 contain the complete DSI Packet Header. The  
 1908 remaining bits, D24 to D63, are informative (shown in yellow in the table) and not relevant to DSI.  
 1909 Therefore, the parity bit calculation can be optimized to:

1910  $P7=0$

1911  $P6=0$

1912  $P5=D10 \wedge D11 \wedge D12 \wedge D13 \wedge D14 \wedge D15 \wedge D16 \wedge D17 \wedge D18 \wedge D19 \wedge D21 \wedge D22 \wedge D23$

1913  $P4=D4 \wedge D5 \wedge D6 \wedge D7 \wedge D8 \wedge D9 \wedge D16 \wedge D17 \wedge D18 \wedge D19 \wedge D20 \wedge D22 \wedge D23$

1914  $P3=D1 \wedge D2 \wedge D3 \wedge D7 \wedge D8 \wedge D9 \wedge D13 \wedge D14 \wedge D15 \wedge D19 \wedge D20 \wedge D21 \wedge D23$

1915  $P2=D0 \wedge D2 \wedge D3 \wedge D5 \wedge D6 \wedge D9 \wedge D11 \wedge D12 \wedge D15 \wedge D18 \wedge D20 \wedge D21 \wedge D22$

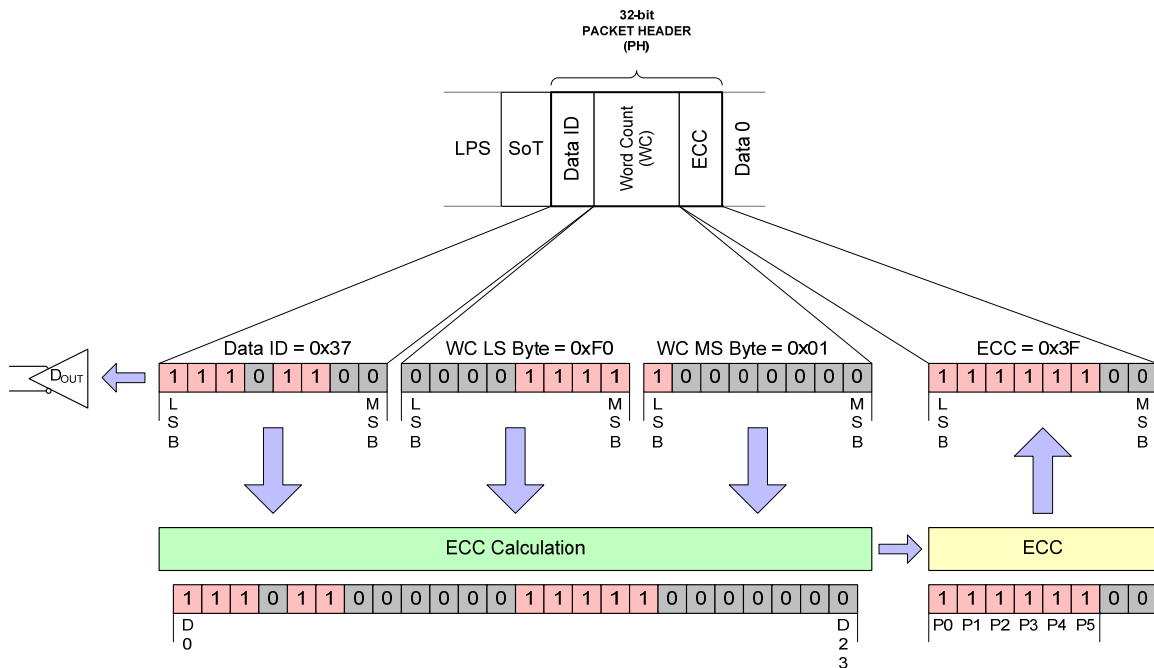
1916  $P1=D0 \wedge D1 \wedge D3 \wedge D4 \wedge D6 \wedge D8 \wedge D10 \wedge D12 \wedge D14 \wedge D17 \wedge D20 \wedge D21 \wedge D22 \wedge D23$

1917  $P0=D0 \wedge D1 \wedge D2 \wedge D4 \wedge D5 \wedge D7 \wedge D10 \wedge D11 \wedge D13 \wedge D16 \wedge D20 \wedge D21 \wedge D22 \wedge D23$

1918 Note, the parity bits relevant to the ECC calculation, P0 through P5, in the table are shown in red and the  
 1919 unused bits, P6 and P7, are shown in blue.

1920 **9.4 ECC Generation on the Transmitter**

1921 ECC is generated from the twenty-four data bits within the Packet Header as illustrated in Figure 33, which  
 1922 also serves as an ECC calculation example. Note that the DSI protocol uses a four byte Packet Header. See  
 1923 section 8.4.1 and section 8.4.2 for Packet Header descriptions for Long and Short packets, respectively.



1924  
 1925

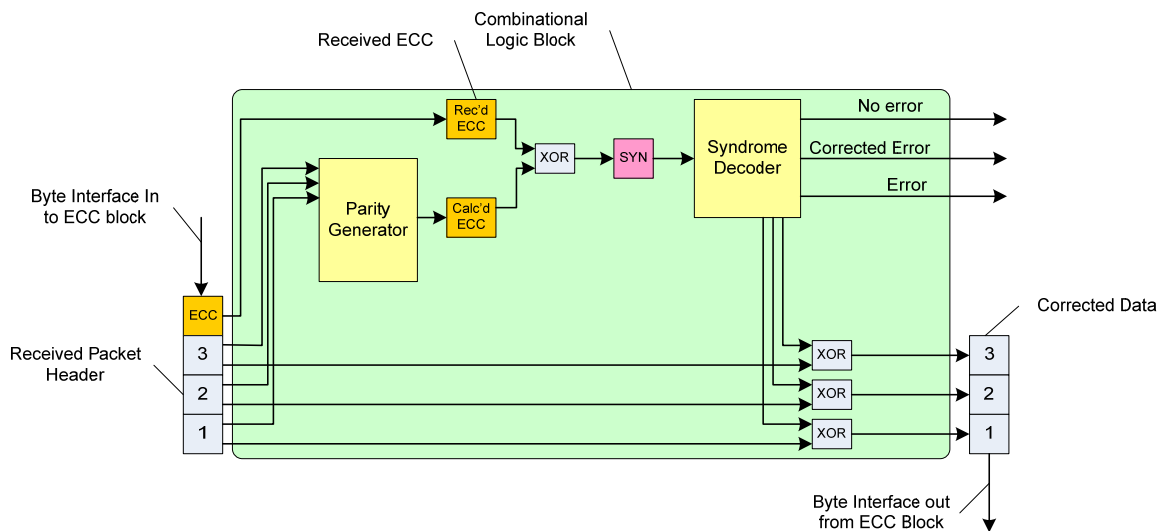
1926

**Figure 33 24-bit ECC generation on TX side**

## 1927 9.5 Applying ECC on the Receiver

1928 Applying ECC on the receiver involves generating a new ECC for the received packet, computing the  
 1929 syndrome using the new ECC and the received ECC, decoding the syndrome to find if a single-error has  
 1930 occurred and if so, correcting the error. If a multiple-bit error is identified, it is flagged and reported to the  
 1931 transmitter. Note, error reporting is only applicable to bidirectional DSI implementations.

1932 ECC generation on the receiver side shall apply the same padding rules as ECC generation for  
 1933 transmission.



1934

1935

**Figure 34 24-bit ECC on RX Side Including Error Correction**

1936 Decoding the syndrome has three aspects:

- 1937 • Testing for errors in the Packet Header. If syndrome = 0, no errors are present.
- 1938 • Test for a single-bit error in the Packet Header by comparing the generated syndrome with the  
 1939 matrix in Table 21. If the syndrome matches one of the entries in the table, then a single-bit error  
 1940 has occurred and the corresponding bit is in error. This position in the Packet Header shall be  
 1941 complemented to correct the error. Also, if the syndrome is one of the rows of the identity matrix  
 1942 **I**, then a parity bit is in error. If the syndrome cannot be identified then a multi-bit error has  
 1943 occurred. In this case the Packet Header is corrupted and cannot be restored. Therefore, the Multi-  
 1944 bit Error Flag shall be set.
- 1945 • Correcting the single-bit error if detected, as indicated above.

## 1946 9.6 Checksum Generation for Long Packet Payloads

1947 Long packets are comprised of a Packet Header protected by an ECC byte as specified in sections 9.3  
 1948 through 9.5, and a payload of 0 to  $2^{16} - 1$  bytes. To detect errors in transmission of Long packets, a  
 1949 checksum is calculated over the payload portion of the data packet. Note that, for the special case of a zero-  
 1950 length payload, the 2-byte checksum is set to 0xFFFF.

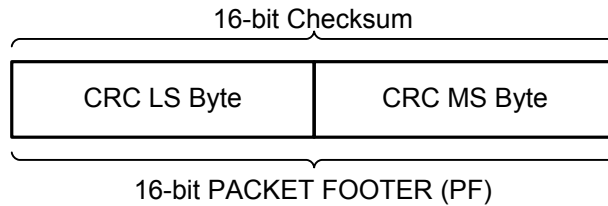
1951 The checksum can only indicate the presence of one or more errors in the payload. Unlike ECC, the  
 1952 checksum does not enable error correction. For this reason, checksum calculation is not useful for  
 1953 unidirectional DSI implementations since the peripheral has no means of reporting errors to the host  
 1954 processor.

1955 Checksum generation and transmission is mandatory for host processors sending Long packets to  
 1956 peripherals. It is optional for peripherals transmitting Long packets to the host processor. However, the  
 1957 format of Long packets is fixed; peripherals that do not support checksum generation shall transmit two  
 1958 bytes having value 0x0000 in place of the checksum bytes when sending Long packets to the host  
 1959 processor.

1960 The host processor shall disable checksum checking for received Long packets from peripherals that do not  
 1961 support checksum generation.

1962 The checksum shall be realized as a 16-bit CRC with a generator polynomial of  $x^{16}+x^{12}+x^5+x^0$ .

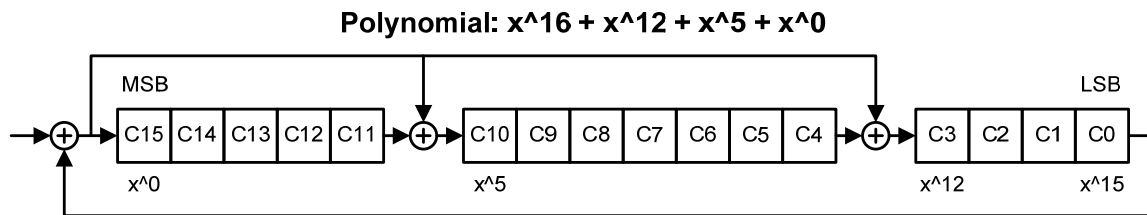
1963 The transmission of the checksum is illustrated in Figure 35. The LS byte is sent first, followed by the MS  
 1964 byte. Note that within the byte, the LS bit is sent first.



1965  
 1966

**Figure 35 Checksum Transmission**

1967 The CRC implementation is presented in Figure 36. The CRC shift register shall be initialized to 0xFFFF  
 1968 before packet data enters. Packet data not including the Packet Header then enters as a bitwise data stream  
 1969 from the left, LS bit first. Each bit is fed through the CRC shift register before it is passed to the output for  
 1970 transmission to the peripheral. After all bytes in the packet payload have passed through the CRC shift  
 1971 register, the shift register contains the checksum. C15 contains the checksum's MSB and C0 the LSB of the  
 1972 16-bit checksum. The checksum is then appended to the data stream and sent to the receiver. The receiver  
 1973 uses its own generated CRC to verify that no errors have occurred in transmission. See Annex B for an  
 1974 example of checksum generation.



1975  
 1976  
 1977

**Figure 36 16-bit CRC Generation Using a Shift Register**

1978 Section 8.10.1 documents the peripheral response to detection of an error in a Long packet payload.  
 1979

## 1980 **10 Compliance, Interoperability, and Optional Capabilities**

1981 This section documents requirements and classifications for MIPI-compliant host processors and  
 1982 peripherals. There are a number of categories of potential differences or attributes that shall be considered  
 1983 to ensure interoperability between a host processor and a peripheral, such as a display module:

1984 Manufacturers shall document a DSI device's capabilities and specifications for the parameters listed in this  
 1985 section.

- 1986 1. Display Resolutions
- 1987 2. Pixel Formats
- 1988 3. Number of Lanes
- 1989 4. Maximum Lane Frequency
- 1990 5. Bidirectional Communication and Escape Mode Support
- 1991 6. ECC and Checksum capabilities
- 1992 7. Display Architecture
- 1993 8. Multiple Peripheral Support

1994 EoTp support and interoperability between DSI v1.01-compliant and earlier revision devices are discussed  
 1995 in section 10.9.

1996 In general, the peripheral chooses one option from each category in the list above. For example, a display  
 1997 module may implement a resolution of 320x240 (QVGA), a pixel format of 16-bpp and use two Lanes to  
 1998 achieve its required bandwidth. Its data path has bidirectional capability, it does not implement  
 1999 checksum-testing capability, and it operates in Video Mode only.

### 2000 **10.1 Display Resolutions**

2001 Host processors shall implement one or more of the display resolutions in Table 23.

2002

**Table 23 Display Resolutions**

Resolution	Horizontal Extent	Vertical Extent
QQVGA	160	120
QCIF	176	144
QCIF+	176	208
QCIF+	176	220
QVGA	320	240
CIF	352	288
CIF+	352	416

Resolution	Horizontal Extent	Vertical Extent
CIF+	352	440
(1/2)VGA	320	480
(2/3)VGA	640	320
VGA	640	480
WVGA	800	480
SVGA	800	600
XVGA	1024	768

2003 **10.2 Pixel Formats**

2004 Pixel formats for Video Mode and Command Mode are defined in the following sections.

2005 **10.2.1 Video Mode**

2006 Peripherals shall implement at least one of the following pixel formats. Host processors shall implement all  
2007 of the following pixel formats; all other Video Mode formats in section 8.8 are optional:

- 2008 1. 16 bpp (5, 6, 5 RGB), each pixel using two bytes; see section 8.8.20
- 2009 2. 18 bpp (6, 6, 6 RGB) packed; see section 8.8.21
- 2010 3. 18 bpp (6, 6, 6 RGB) loosely packed into three bytes; see section 8.8.22
- 2011 4. 24 bpp (8, 8, 8 RGB), each pixel using three bytes; see section 8.8.23

2012 **10.2.2 Command Mode**

2013 Peripherals shall implement at least one of the pixel formats, and host processors should implement all of  
2014 the pixel formats, defined in [MIPI01].

2015 **10.3 Number of Lanes**

2016 In normal operation a peripheral uses the number of Lanes required for its bandwidth needs.

2017 The host processor shall implement a minimum of one Data Lane; additional Lane capability is optional. A  
2018 host processor with multi-Lane capability (N Lanes) shall be able to operate with any number of Lanes  
2019 from one to N, to match the fixed number of Lanes in peripherals using one to N Lanes. See section 6.1 for  
2020 more details.

2021 **10.4 Maximum Lane Frequency**

2022 The maximum Lane frequency shall be documented by the DSI device manufacturer. The Lane frequency  
2023 shall adhere to the specifications in [MIPI04].

## 2024 **10.5 Bidirectional Communication**

2025 Because Command Mode depends on the use of the READ command, a Command Mode display module  
2026 shall implement bidirectional communications. For display modules without on-panel buffers that work  
2027 only in Video Mode, bidirectional operation on DSI is optional.

2028 Since a host processor may implement both Command- and Video Modes of operations, it should support  
2029 bidirectional operation and Escape Mode transmission and reception.

## 2030 **10.6 ECC and Checksum Capabilities**

2031 A DSI host processor shall calculate and transmit an ECC byte for both Long and Short packets. The host  
2032 processor shall also calculate and transmit a two-byte Checksum for Long packets. A DSI peripheral shall  
2033 support ECC, but may support Checksum. If a peripheral does not calculate Checksum it shall still be  
2034 capable of receiving Checksum bytes from the host processor. If a peripheral supports bidirectional  
2035 communications and does not support Checksum it shall send bytes of all zeros in the appropriate fields.  
2036 For interoperability with earlier revision of DSI peripherals where ECC was considered an optional feature,  
2037 host shall be able to enable/disable ECC capability based on the particular peripheral ECC support  
2038 capability. The enabling/disabling mechanism is out of scope of DSI. In effect, if an earlier revision  
2039 peripheral was not supporting ECC, it shall still be capable of receiving ECC byte from the host and  
2040 sending an all zero ECC byte back to the host for responses over a bidirectional link. See section 9 for more  
2041 details on ECC and Checksum.

## 2042 **10.7 Display Architecture**

2043 A display module may implement Type 1, Type 2, Type 3 or Type 4 display architecture as described in  
2044 [MIPI02] and [MIPI03]. Type 1 architecture works in Command Mode only. Type 2 and Type 3  
2045 architectures use the DSI interface for both Command- and Video Modes of operation. Type 4 architectures  
2046 operate in Video Mode only, although there may be additional control signals. Therefore, a peripheral may  
2047 use Command Mode only, Video Mode only, or both Command- and Video Modes of operation.

2048 The host processor may support either or both Command- and Video Modes of operation. If the host  
2049 processor supports Command Mode, it shall also support the mandatory command set specified in  
2050 [MIPI01].

## 2051 **10.8 Multiple Peripheral Support**

2052 DSI supports multiple peripherals per DSI Link using the Virtual Channel field of the Data Identifier byte.  
2053 See sections 4.2.3 and 8.5.1 for more details.

2054 A host processor should support a minimum of two peripherals.

## 2055 **10.9 EoTp Support and Interoperability**

2056 EoTp generation or detection is mandatory for devices compliant with this version of the DSI specification.  
2057 Devices compliant to DSI specification v1.0 and earlier do not support EoTp. In order to ensure  
2058 interoperability with earlier devices, current devices shall provide a means to enable or disable EoTp  
2059 generation or detection. In effect, this capability can be disabled by the system designer whenever a device  
2060 on either side of the Link does not support EoTp.  
2061

## 2062 **Annex A Contention Detection and Recovery Mechanisms (informative)**

2063 The following describes optional capabilities at the PHY and Protocol layers that provide additional  
 2064 robustness for a DSI Link against possible data-signal contention as a consequence of transient errors in the  
 2065 system. These capabilities improve the system's chances of detecting any of several possible contention  
 2066 cases, and provide mechanisms for "graceful" recovery without resorting to a hard reset.

2067 These capabilities combine circuitry in the I/O cell, to directly detect contention, with logic and timers in  
 2068 the protocol to avert and recover from other forms of contention.

### 2069 **A.1 PHY Detected Contention**

2070 The PHY can detect two types of contention faults: LP High Fault and LP Low Fault.

2071 The LP High Fault and LP Low Fault are caused by both sides of the Link transmitting simultaneously.  
 2072 Note, the LP High Fault and LP Low Fault are only applicable for bidirectional Data Lanes. Refer to  
 2073 [MIPI04] for definition of LP High and LP Low faults.

#### 2074 **A.1.1 Protocol Response to PHY Detected Faults**

2075 The Protocol shall specify how both ends of the Link respond when contention is flagged. It shall ensure  
 2076 that both devices return to *Stop* state (LP-11), with one side going to *Stop TX* and the other to *Stop RX*.

2077 When both PHYs are in LP mode, one or both PHYs will detect contention between LP-0 and LP-1.

2078 The following tables describe the resolution sequences for different types of contention and detection.

2079 Table sequences:

- 2080 • Sequence of events to resolve LP High  $\leftrightarrow$  LP Low Contention
- 2081 • Case 1: Both sides initially detect the contention
- 2082 • Case 2: Only the Host Processor initially detects contention
- 2083 • Case 3: Only the Peripheral initially detects contention

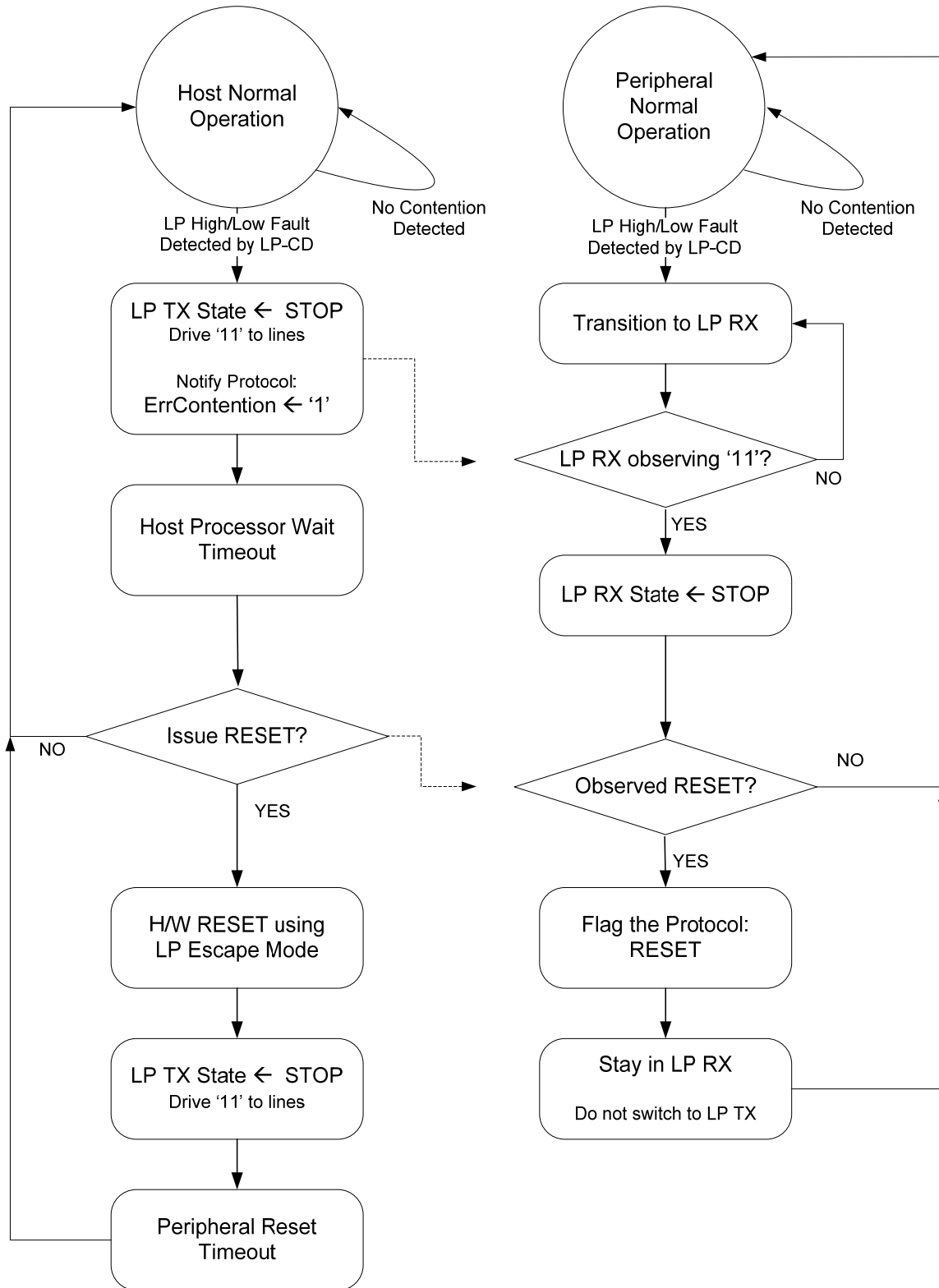
2084 **Table 24 LP High  $\leftrightarrow$  LP Low Contention Case 1**

Host Processor Side		Peripheral Side	
Protocol	PHY	PHY	Protocol
	Detect <i>LP High Fault</i> or <i>LP Low Fault</i>	Detect <i>LP High Fault</i> or <i>LP Low Fault</i>	
	Transition to <i>Stop</i> State (LP-11)	Transition to LP-RX	Set <i>Contention Detected</i> in Error Report (see Table 18)
Host Processor Wait Timeout		Peripheral waits until it observes <i>Stop</i> state before responding	
		Observe <i>Stop</i> state	
Request Reset Entry Command to PHY (optional)	Send Reset Entry Command	Observe Reset Entry Command	

Host Processor Side		Peripheral Side	
Protocol	PHY	PHY	Protocol
		Flag Protocol about Reset Command	Observe Reset Entry Command
			Reset Peripheral
	Return to Stop State (LP-11)	Remain in LP-RX	(reset may continue)
Peripheral Reset Timeout. Wait until Peripheral completes Reset before resuming normal operation.	Continue normal operation.		Reset completes

2085 Note: The protocol may want to request a Reset after contention is flagged a single time. Alternately, the  
 2086 protocol may choose not to Reset but instead continue normal operation after detecting a single contention.  
 2087 It could then initiate a Reset after multiple contentions are flagged, or never initiate a Reset.





2088  
2089

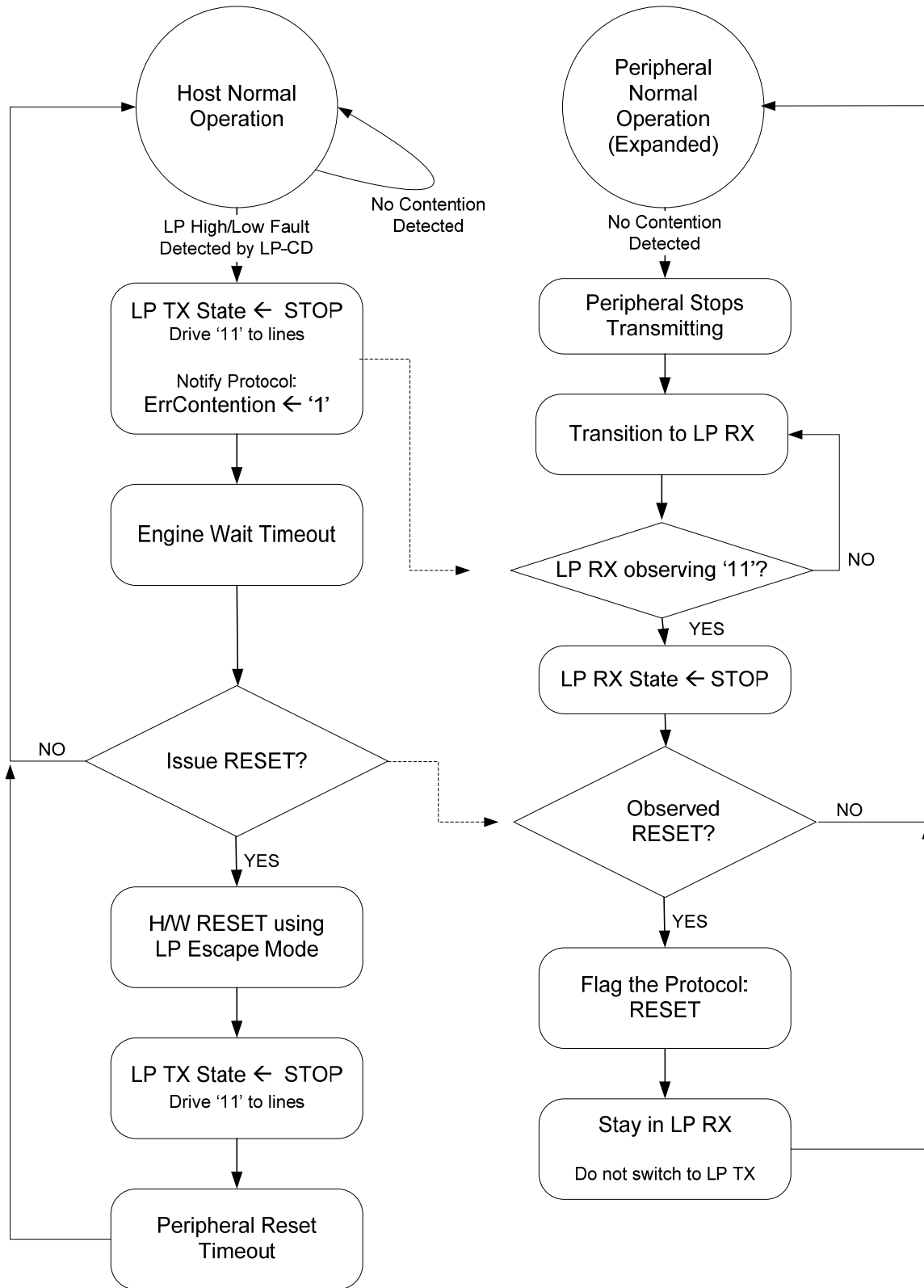
2090

**Figure 37 LP High ↔ LP Low Contention Case 1**

2091

**Table 25 LP High ↔ LP Low Contention Case 2**

Host Processor Side		Peripheral Side	
Protocol	PHY	PHY	Protocol
	Detect <i>LP High Fault</i> or <i>LP Low Fault</i>	No EL contention detected	
	Transition to <i>Stop State</i> (LP-11)	No EL contention detected	
Host Processor Wait Timeout			Peripheral Bus Possession Timeout
		Transition to LP-RX	
		Observe <i>Stop state</i>	
Request <i>Reset Entry</i> command to PHY	Send <i>Reset Entry</i> command	Observe <i>Reset Entry</i> command	
		Flag Protocol: <i>Reset</i> command received	Observe <i>Reset Command</i>
			Reset Peripheral
	Return to <i>Stop state</i> (LP-11)	Remain in LP-RX	(reset continues)
Peripheral Reset Timeout. Wait until peripheral completes Reset before resuming normal operation.	Continue normal operation.		Reset completes



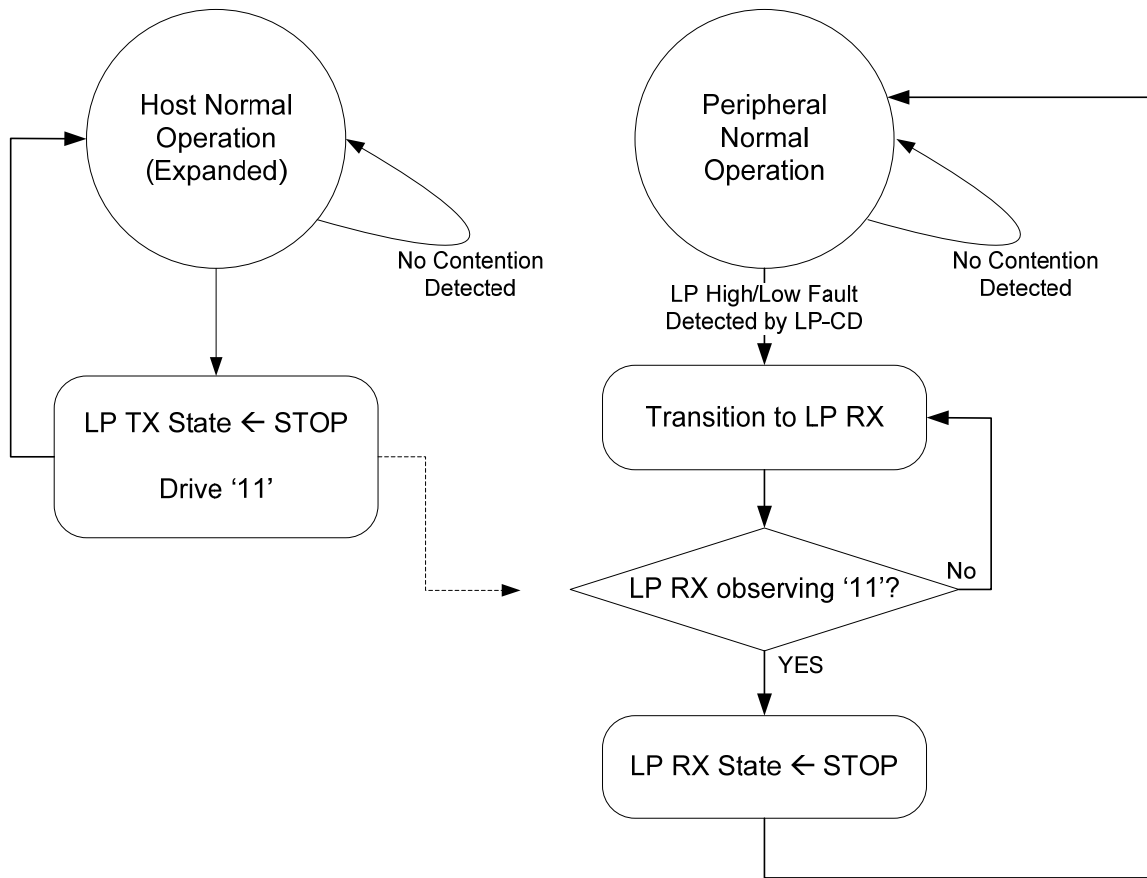
2092  
2093

**Figure 38 LP High ↔ LP Low Contention Case 2**

2094

**Table 26 LP High ↔ LP Low Contention Case 3**

Host Processor Side		Peripheral Side	
Protocol	PHY	PHY	Protocol
	No detection of EL contention	Detect <i>LP High Fault</i> or <i>LP Low Fault</i>	
		Transition to LP-RX	Set <i>Contention Detected</i> in Error Report (see Table 18)
		Peripheral waits until it observes <i>Stop</i> state before responding to bus activity.	
	Normal transition to <i>Stop</i> State (LP-11)	Observe <i>Stop</i> State	



2095

2096

2097

**Figure 39 LP High ↔ LP Low Contention Case 3**

2098 **Annex B Checksum Generation Example (informative)**

2099 The following C/C++ program provides a simple software routine to calculate CRC of a packet of variable  
 2100 length. The main routine calls subroutine CalculateCRC16 to calculate the CRC based on the data in  
 2101 one of the gpcTestData[ ] arrays and prints the CRC results.

2102

```

2103 /* ***** DECLARATIONS ***** */
2104 #include <stdio.h>
2105
2106 /* Start of Test Data */
2107 static unsigned char gpcTestData0[] = { 0x00 };
2108 static unsigned char gpcTestData1[] = { 0x01 };
2109 static unsigned char gpcTestData2[] = { 0xFF, 0x00, 0x00, 0x00, 0x1E,
2110     0xF0, 0x1E, 0xC7, 0x4F, 0x82, 0x78, 0xC5, 0x82, 0xE0, 0x8C, 0x70,
2111     0xD2, 0x3C, 0x78, 0xE9, 0xFF, 0x00, 0x00, 0x01 };
2112 static unsigned char gpcTestData3[] = { 0xFF, 0x00, 0x00, 0x02, 0xB9,
2113     0xDC, 0xF3, 0x72, 0xBB, 0xD4, 0xB8, 0x5A, 0xC8, 0x75, 0xC2, 0x7C,
2114     0x81, 0xF8, 0x05, 0xDF, 0xFF, 0x00, 0x00, 0x01 };
2115 #define NUMBER_OF_TEST_DATA0_BYTES 1
2116 #define NUMBER_OF_TEST_DATA1_BYTES 1
2117 #define NUMBER_OF_TEST_DATA2_BYTES 24
2118 #define NUMBER_OF_TEST_DATA3_BYTES 24
2119 /* End of Test Data */
2120
2121 unsigned short CalculateCRC16( unsigned char *pcDataStream, unsigned
2122 short sNumberOfDataBytes );
2123
2124 /* ***** MAIN ROUTINE ***** */
2125 void main( void )
2126 {
2127     unsigned short sCRC16Result;
2128     sCRC16Result = CalculateCRC16( gpcTestData2,
2129         NUMBER_OF_TEST_DATA2_BYTES );
2130     printf( "Checksum CS[15:0] = 0x%04X\n", sCRC16Result );
2131 }
2132 /* ***** END OF MAIN ***** START OF CRC CALCULATION ***** */
2133
2134 /* CRC16 Polynomial, logically inverted 0x1021 for x^16+x^15+x^5+x^0 */
2135 static unsigned short gsCRC16GenerationCode = 0x8408;
2136
2137 unsigned short CalculateCRC16( unsigned char *pcDataStream, unsigned
2138 short sNumberOfDataBytes )
2139 {
2140     /*
2141     sCRC16Result: the return of this function,
2142     sByteCounter: address pointer to count the number of the
2143     calculated data bytes
2144     cBitCounter: counter for bit shift (0 to 7)
2145     cCurrentData: byte size buffer to duplicate the calculated data
2146     byte for a bit shift operation
2147     */
2148     unsigned short sByteCounter;
  
```

```

2149     unsigned char cBitCounter;
2150     unsigned char cCurrentData;
2151     unsigned short sCRC16Result = 0xFFFF;
2152     if ( sNumberOfDataBytes > 0 )
2153     {
2154         for ( sByteCounter = 0; sByteCounter < sNumberOfDataBytes;
2155              sByteCounter++ )
2156         {
2157             cCurrentData = *( pcDataStream + sByteCounter );
2158             for ( cBitCounter = 0; cBitCounter < 8;
2159                  cBitCounter++ )
2160             {
2161                 if ( ( ( sCRC16Result & 0x0001 ) ^ ( ( 0x0001 *
2162                  cCurrentData) & 0x0001 ) ) > 0 )
2163                     sCRC16Result = ( ( sCRC16Result >> 1 )
2164                      & 0x7FFF ) ^ gsCRC16GenerationCode;
2165                 else
2166                     sCRC16Result = ( sCRC16Result >> 1 )
2167                      & 0x7FFF;
2168                 cCurrentData = ( cCurrentData >> 1 ) & 0x7F;
2169             }
2170         }
2171     }
2172     return sCRC16Result;
2173 }
2174 /* ***** END OF SUBROUTINE TO CALCULATE CRC ***** */

```

2175 Outputs from the various input streams are as follows:

2176 Data (gpcTestData0): 00

2177 Checksum CS[15:0] = 0x0F87

2178 Data (gpcTestData1): 01

2179 Checksum CS[15:0] = 0x1E0E

2180 Data (gpcTestData2): FF 00 00 00 1E F0 1E C7 4F 82 78 C5 82 E0 8C 70 D2 3C  
2181 78 E9 FF 00 00 01

2182 Checksum CS[15:0] = 0xE569

2183 Data (gpcTestData3): FF 00 00 02 B9 DC F3 72 BB D4 B8 5A C8 75 C2 7C 81 F8  
2184 05 DF FF 00 00 01

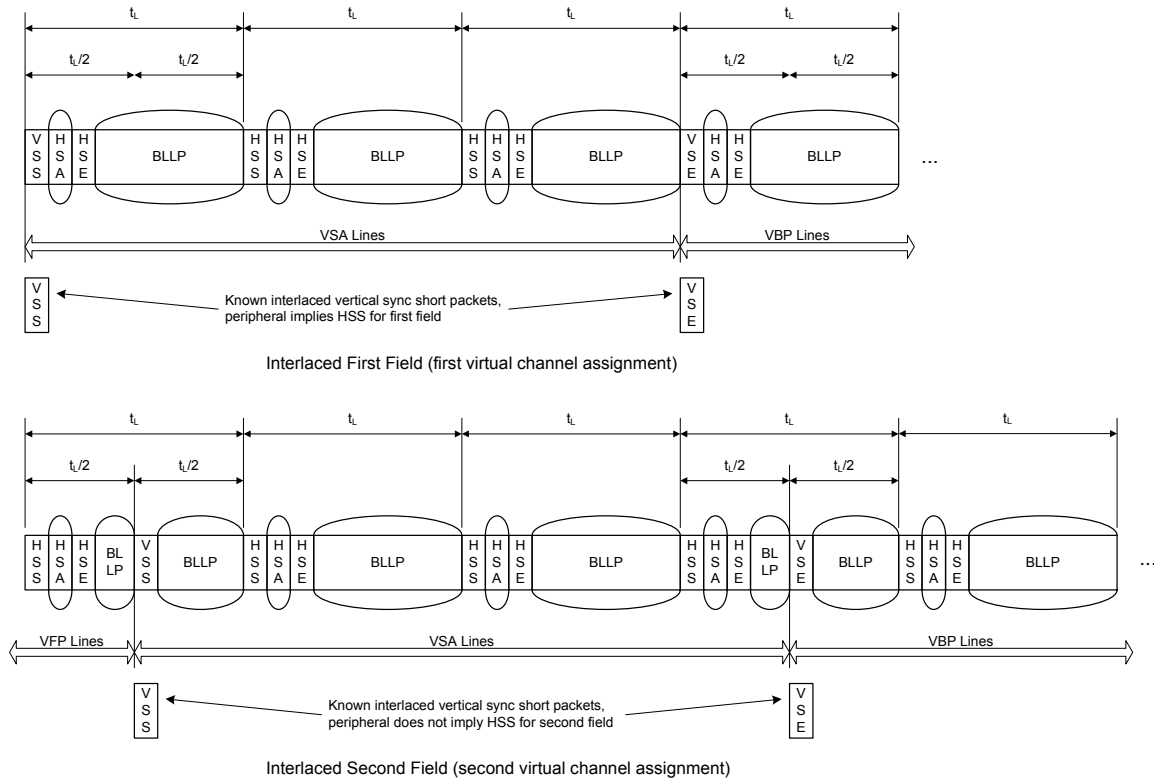
2185 Checksum CS[15:0] = 0x00F0

2186

2187 **Annex C Interlaced Video Transmission Sourcing**

2188 In this annex, the diagrams are normative only in the sense that they are defining a method of transporting  
 2189 interlaced video with this specification. The use of interlaced video and its support by host, display module  
 2190 or other peripheral is optional.

2191 An example of the video mode interface timing for non-burst transmission with Sync Start and End  
 2192 sourcing interlaced video is shown in Figure 40. Note that in the first field, no timing differs from Figure  
 2193 30. In the second field, note HSS is not implied at the V Sync Start and V Sync End timing pulses.



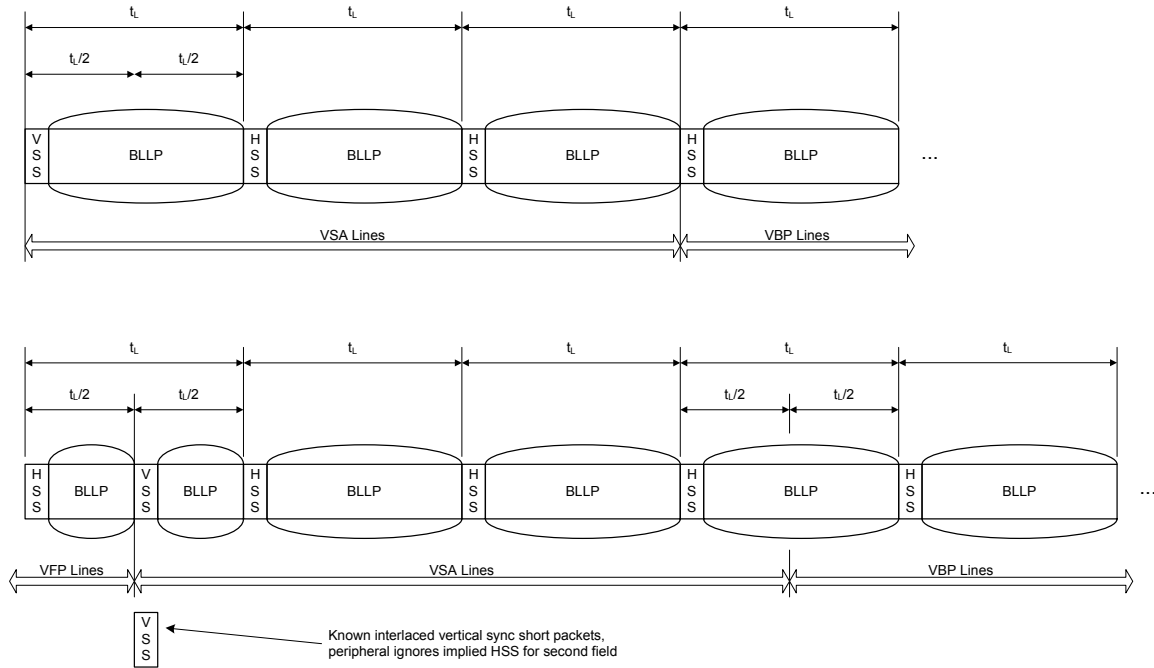
2194

2195

2196

**Figure 40 Video Mode Interface Timing: Non-burst Transmission with Sync Start and End (Interlaced Video)**

2197 An example of the video mode interface timing for non-burst transmission with Sync Events sourcing  
 2198 interlaced video is shown in Figure 41. Note that in the first field, no timing differs from the previous  
 2199 example. In the second field, note HSS is not implied at the V Sync Start timing event.



2200

2201

2202

**Figure 41 Video Mode Interface Timing: Non-burst Transmission with Sync Events (Interlaced Video)**